Unified Patent Court
Einheitliches Patentgericht
Juridiction unifiée du brevet

EPG – Court of Appeal
UPC_CoA_764/2024
UPC_CoA_774/2024

DECISION

of the Court of Appeal of the Unified Patent Court issued on 2 October 2025

HEADNOTE

- An inadmissible extension of the subject matter exists if the subject matter of the granted claim goes beyond the content of the application as originally filed. In order to determine this, the court must first ascertain what information a person skilled in the art, based on an objective assessment and referring to the filing date, would immediately and unambiguously derive from the entirety of the application as filed, using their general technical knowledge. In doing so, implicitly disclosed subject matter must also be considered part of the content, i.e. subject matter that clearly and unambiguously follows from what is expressly stated.

- If, as in this case, the patent has been derived from a divisional application, this requirement applies to each earlier application. The subject matter of the granted claim 1 must therefore not go beyond (1) the disclosure of the originally filed application for the contested patent and (2) the disclosure of the original PCT application which entered the regional phase and constitutes the parent application of the divisional application.

KEYWORDS

unacceptable extension

APPELLANTS (AND DEFENDANTS BEFORE THE COURT OF FIRST INSTANCE)

1. **expert e-Commerce GmbH**, Langenhagen, Germany
2. **expert klein GmbH**, Burbach, Germany

hereinafter referred to collectively as 'expert' and individually as 'expert e-Commerce' and 'expert klein'

represented by Dr Dirk Jestaedt, lawyer, KRIEGER MES Partnerschaft mbB, Düsseldorf, Germany, supported by European Patent Attorney Bernhard Ganahl, HGF Europe LLP, Munich, Germany

RESPONDENT (AND APPLICANT BEFORE THE COURT OF FIRST INSTANCE)

Seoul Viosys Co., Ltd., Danwon-gu, Ansan-si, Gyeonggi-do, 15429, Republic of

Korea hereinafter referred to as 'Viosys'

represented by Dr Bolko Ehlgen, lawyer, and other lawyers from the law firm Linklaters LLP, Frankfurt am Main, Germany, supported by Dr Dipl.-Phys. Olaf Isfort, European Patent Attorney, Schneiders & Behrendt, Frankfurt am Main, Germany

INTERVENER ON THE SIDE OF THE RESPONDENT (AND PLAINTIFF BEFORE THE COURT OF FIRST INSTANCE)

Seoul Semiconductor Co., Ltd., Danwon-gu, Ansan-si, Gyeonggi-do, 15429, Republic of Korea

represented by Dr Bolko Ehlgen and other lawyers from the law firm Linklaters LLP, Frankfurt am Main, Germany

LANGUAGE OF THE PROCEEDINGS

German. With the consent of the parties, the oral proceedings were conducted in a hybrid form, with both German and English being permitted.

PATENT IN CONTENTION EP 3 926 698

ADJUDICATING BODY AND PRESIDING JUDGES

This order was issued by Panel 2:
Rian Kalden, presiding judge and rapporteur Patricia Rombach, legally qualified judge Ingeborg Simonsson, legally qualified judge Torsten Duhme, technically qualified judge
Max Tilmann, technically qualified judge

CONTESTED DECISION OF THE COURT OF FIRST INSTANCE

Local Chamber Düsseldorf, decision of 10 October 2024 Case number of the Court of First Instance:
ORD_598458/2023 in the main proceedings concerning the infringement action, in ACT_579244/2023 UPC_CFI_363/2023,
ORD_50675/2024 in main proceedings concerning the counterclaim for annulment, in CC_3580/2024 UPC_CFI_363/2023

ORAL HEARING

The oral hearing took place on 11 July 2025.
Cases APL_64222/2024 UPC_CoA_764/2024 and APL_64721/2024 UPC_CoA_774/2024 are being heard jointly (R.302.3 RPP).

PRESENTATION OF THE FACTS

The parties

1. expert klein is part of the expert retail group, which operates in 22 countries in the fields of consumer electronics, information technology, telecommunications, entertainment and household appliances. expert klein is responsible in particular for the online presence and e-commerce activities of the expert group in Germany.
2. Expert e-Commerce operates 25 specialist stores on its own behalf as part of the "Expert Specialist Trade Cooperation".
3. Online sales (among other things) of the contested embodiment are carried out jointly by both defendants.
4. Viosys is a global full-service provider of LEDs and vertical cavity surface emitting lasers.

The patent in dispute

5. Viosys is the owner of the patent in dispute (hereinafter also referred to as "the patent"), which relates to a light-emitting diode (hereinafter also referred to as "LED"). The patent is based on a divisional application of European patent application number 17165501.2 (which led to EP 3 223 320, hereinafter: EP320), which in turn is a divisional application of European patent application number 12832213.8 (submitted as Annex B5), which was published as EP 2 757 598 A2 in accordance with Art. 153(4) EPC. This application is hereinafter referred to as the parent application. The parent application is the European regional phase of the Korean-language PCT application with application number PCT KR2012/007358. The latter was published under the number WO 2013/039344 A2. The patent claims priority from the Korean applications KR20110093396 of 16 September 2011, KR20120015758 of 16 February 2012 and KR20120052722
   dated 17 May 2012.
6. The notice of patent grant was published on 4 January 2023.
7. The patent is in force in the EPC member states Germany, Austria, Belgium, France, Italy, Luxembourg, the Netherlands and Sweden (hereinafter referred to as "territories").
8. The patent comprises 14 claims. Claim 1 of the contested patent reads as follows:

   "Light-emitting diode comprising:

   a light-emitting structure formed on a substrate (100) and comprising a semiconductor layer (110) of a first conductivity type,
   an active layer (120) and a semiconductor layer (130) of a second conductivity type;

   mesa-etched regions (150) formed from the surface of the semiconductor layer (130) of the second conductivity type
   to the semiconductor layer (110) of the first conductivity type;

   a reflective electrode (140) formed on the semiconductor layer (130) of the second conductivity type
   and comprising a reflective metal layer (142), a metal barrier layer (144) and a relaxation layer (143) formed between the reflective metal layer (142) and the metal barrier layer (144),

wherein the relaxation layer (143) has a thermal expansion coefficient between the thermal expansion coefficient of the reflective metal layer (142) and the thermal expansion coefficient of the metal barrier layer (144);

a lower insulating layer (200) covering a total surface of the structure, which by the semiconductor layer (110) of the first conductivity type, the active layer (120), the semiconductor layer (130) of the second conductivity type, the meso-etched regions (150) and the reflective electrode (140), wherein the lower insulating layer (200) allows an upper surface of the reflective electrode (140) to partially expose through it, and further has openings located near an edge of the substrate that allow the semiconductor layer (110) of the first conductivity type to be exposed through them in the mesa-etched areas (150);

a current expansion layer (210) formed on the lower insulating layer (200), which covers the semiconductor layer (110) of the first conductivity type and is electrically connected to the semiconductor layer (110) of the first conductivity type;

an upper insulating layer (220) formed on the current expansion layer (210), wherein both the current expansion layer (210) and the reflective electrode (140) are partially exposed through the upper insulating layer (220);

a first pad (230) electrically connected to the current expansion layer (210) exposed through the upper insulating layer (220);

and *a second pad (240) electrically connected to the reflective electrode (140) exposed through the upper insulating layer (220);*

9. The invention relates to an LED, and in particular a flip-chip type LED with improved light output (para. [0001]).
10. Under the heading "State of the art", the description explains that LEDs are formed on a substrate and contain an N-type semiconductor layer, a P-type semiconductor layer and an active layer between them. An N-electrode pad is formed on the N-semiconductor layer and a P-electrode pad is formed on the P-semiconductor layer. For operation, the light-emitting diode is electrically connected to an external power source via the electrode pads. At this point, a current flows from the P-electrode pad to the N-electrode pad through the semiconductor layers (para. [0003]).
11. In order to improve heat dissipation and at the same time prevent light loss through the P-electrode pad, an LED with a flip-chip structure is used in the prior art, and various electrode structures have been proposed to support current distribution in a large-area flip-chip type LED. For example, a reflective electrode is formed on the P-type semiconductor layer, and extensions for current propagation are formed on an area of the N-type semiconductor layer exposed by etching the P-type semiconductor layer and the active layer (para. [0004]).

12. Conventional techniques use linear extensions, which restrict current distribution due to their high resistance. Furthermore, since a reflective electrode is only arranged on the P-type semiconductor layer, significant light loss occurs through the pads and extensions instead of being reflected by the reflective electrode (para. [0006]).
13. Under the heading "Technical Problem", the patent specification describes that the invention aims to provide an LED with improved current distribution performance and light extraction efficiency by improving reflectivity (paras. [0014] and [0015]).
14. Under the heading "Technical Solution", it is explained that, according to one aspect of the invention, an LED structure is disclosed which comprises a semiconductor layer of a first conductivity type, an active layer and a semiconductor layer of a second conductivity type. The patent specification then essentially repeats the wording of the above-mentioned claim 1 (para. [0019]). The description goes on to state that, according to a further aspect of the present invention, an LED comprises: a semiconductor layer of a first conductivity type (hereinafter also referred to as the first semiconductor layer); on the first semiconductor layer, a plurality of mesas separated from each other and each having an active layer and a semiconductor layer of a second conductivity type (hereinafter also referred to as the second semiconductor layer); reflective electrodes, each of which is arranged on the corresponding mesa area and is in ohmic contact with the second semiconductor layer; and a current expansion layer covering the plurality of mesas and the first semiconductor layer to be electrically insulated from the mesas, wherein the current expansion layer includes first openings formed in the upper regions of the mesas to expose the reflective electrodes through them, wherein the current expansion layer is further in ohmic contact with the first conductive semiconductor layer (para. [0020]).
15. The patent specification explains that the LED has improved current distribution performance due to the current expansion layer, since the current expansion layer covers the plurality of mesas and the first semiconductor layer ([para. 0021]).
16. Under the heading "Advantageous Effects," the description states that embodiments of the invention can provide an LED, in particular a flip-chip type LED, that has improved current distribution performance. In addition, the LED has improved reflectivity, providing improved light extraction performance. Furthermore, the LED has a simple structure with a plurality of mesas, thereby simplifying the process of manufacturing the LED (para. [0044]).
17. The description then explains the drawings. The patent specification contains 36 figures, of which Figures 6, 7, 10, 11, 12, 14, 18, 19 and 24-26 are shown below.

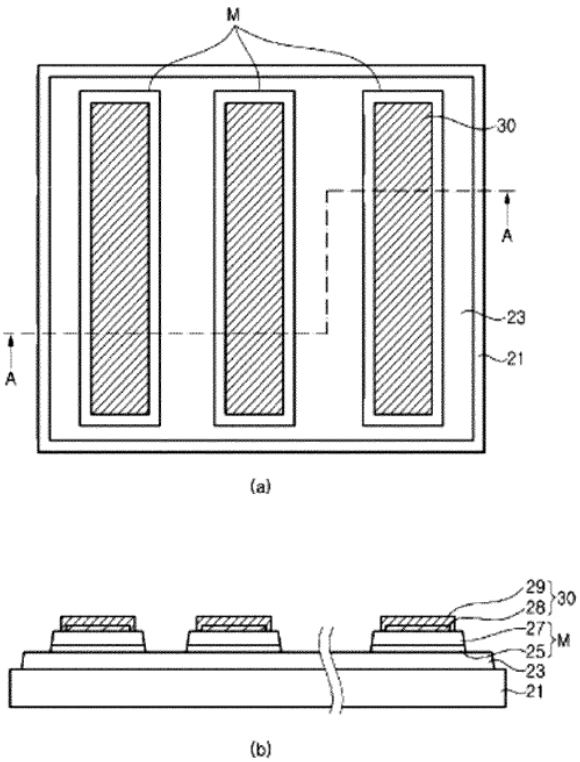


Fig. 6

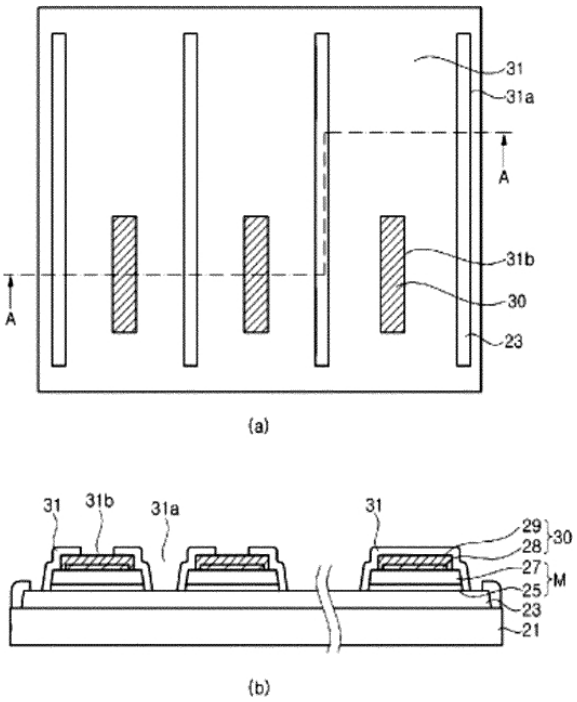


Fig. 7

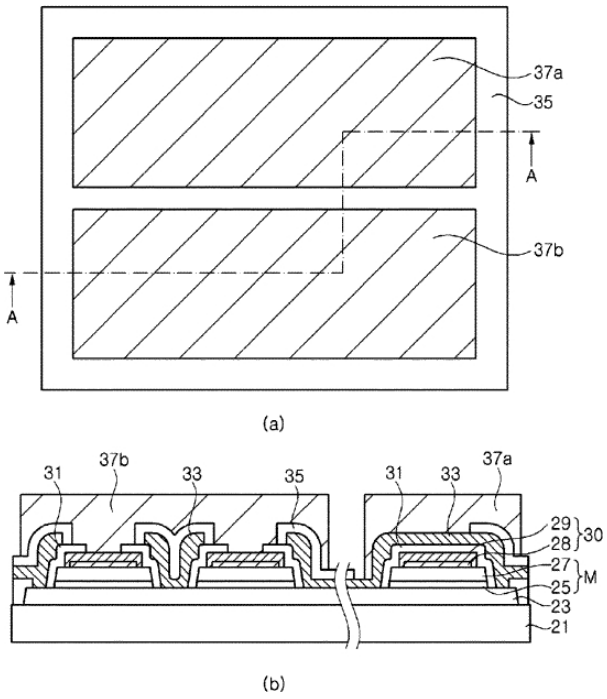


Fig. 10

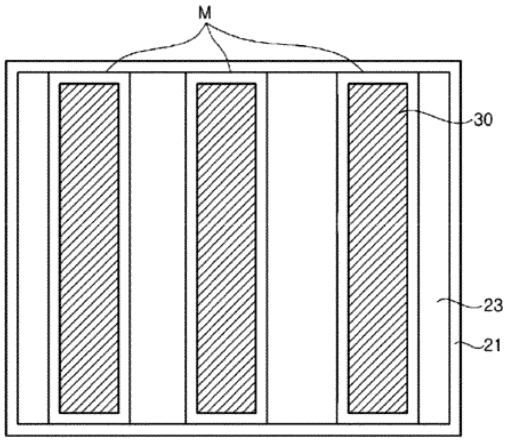


Fig. 11

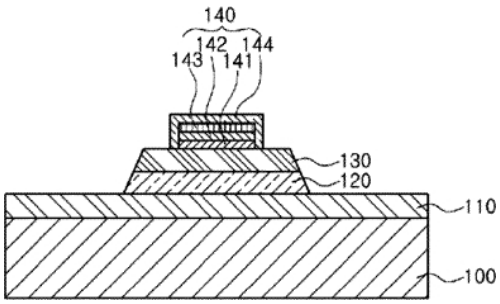


Fig. 12

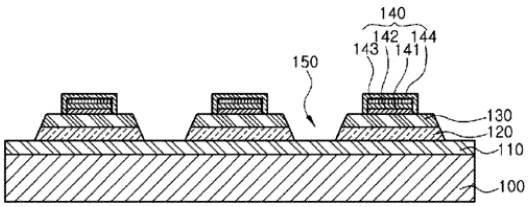


Fig. 14

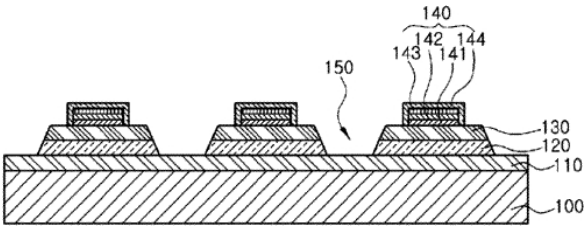


Fig. 18

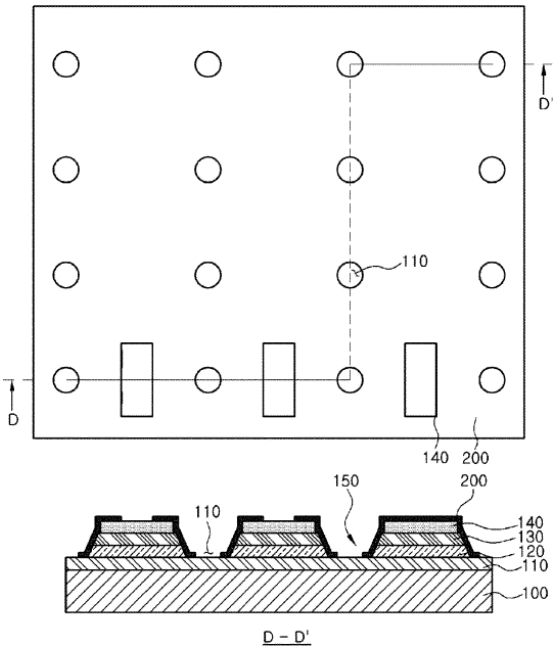


Fig. 19

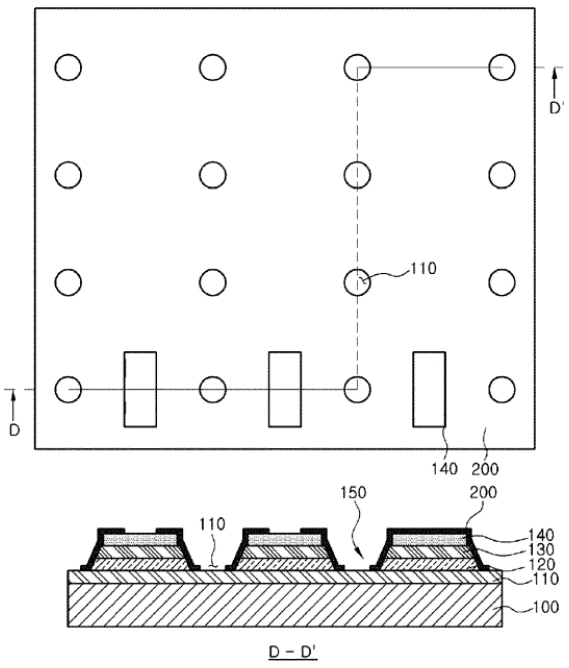


Fig. 24

18. The invention is explained in the description using examples of embodiments. One example is described in paragraphs [0069] to [0085], which describe the following (in summary) with reference to Figure 10:
First, a first semiconductor layer (23) is formed on a substrate (21). A plurality of separate mesas M are formed on the first semiconductor layer by etching. Each of these mesas contains an active layer (25) and a second semiconductor layer (27). The active layer
(25) is arranged between the first (23) and second (27) semiconductor layers. In addition, reflective electrodes (30) are located on each of the plurality of mesas M. The reflective electrode (30) covers most of the top surface of the corresponding mesa M and has essentially the same shape as that of the mesa M in plan view.
A lower insulating layer (31) covers the plurality of mesas M and the first semiconductor layer (23). It has openings (31a) through which the first semiconductor layer (23) is exposed, and openings (31b) through which the reflective electrodes are exposed.
A current expansion layer (33) is formed on the lower insulating layer (31), covering the majority of the mesas M and the first semiconductor layer (23). The current expansion layer (33) has openings (33a) through which the reflective electrodes are exposed. Through the openings (31a) of the lower insulating layer (31), the current expansion layer (33) can be in ohmic contact with the first semiconductor layer (23).
An upper insulating layer (35) with openings (35a) and (35b) is formed on the current expansion layer (33). Pads (37a) and (37b) are formed on the upper insulating layer, wherein the first pad (37a) is connected to the current expansion layer (33) via the openings (35a) and the second pad (37b) is connected to the reflective electrodes via the openings (35b).

The contested embodiment in the infringement action

19. Viosys claims that the SMART.5 32 GB smartphone manufactured by emporia telecom GmbH + Co KG (Austria) and distributed by expert contains a single LED chip (which is installed in connection with the camera module of this smartphone) that infringes the patent.

Background to the proceedings and contested decision

20. Viosys filed an infringement action with the Local Chamber Düsseldorf of the EPG (hereinafter: LKD).
21. expert klein filed a counterclaim for annulment together with its statement of defence. Viosys then requested an amendment to the patent based on several auxiliary requests.
22. In the contested decision, the LKD found that the priority date of the patent was 17 May 2012, as the patent could not claim the priorities of the two earlier Korean applications. It further found that the patent did not suffer from an impermissible extension of the subject matter nor was it obvious, as claimed by expert klein, and that the contested embodiment infringed the patent. Among other things, the LKD issued a cease-and-desist order, imposing a penalty payment in the event of non-compliance.
23. expert lodged an appeal in good time.

SUMMARY OF THE PARTIES' SUBMISSIONS:

24. expert requests that the Court of Appeal (1) set aside the contested decision concerning the infringement action and dismiss the infringement action, and (2) order Viosys to pay the costs.
25. expert klein requests that the Court of Appeal (1) set aside the contested decision concerning the counterclaim for revocation and declare claims 1, 4, 5, 6 and 9 invalid with effect for the territories, and (2) order Viosys to pay the costs.

26. Viosys requests that (1) the appeals be dismissed, alternatively on the basis of the patent as maintained in accordance with an auxiliary request, and (2) expert be ordered to pay the costs of the appeal proceedings.

SUMMARY OF THE PARTIES' ARGUMENTS

27. expert challenges the LKD's decision in its entirety. expert argues that, while the LKD correctly found that the patent covers embodiments with only one mesa, it erred in finding that claim 1 was sufficiently disclosed in Figures 24 to 26 of the parent application. However, since the LKD based its opinion on the fact that claim 1 was sufficiently disclosed in Figures 24 to 26 of the parent application, it wrongly found that this embodiment disclosed all the features of the contested patent, including feature 5.2. Expert also disagrees with the LKD's assessment that the invention protected by the patent is not obvious, as well as with its finding that the contested embodiment infringes the patent.
28. Viosys defends the contested decision.

REASONS FOR THE DECISION

Person skilled in the art

29. It is undisputed that the relevant skilled person is a graduate engineer or a person with a master's degree in electrical engineering or semiconductor physics with a technical college degree and several years of professional experience in the development of light-emitting diodes (LEDs) and methods for their manufacture.

Interpretation of the claims

30. For the sake of simplicity, the features of claim 1 can be broken down as follows:

1. A **light-emitting diode** comprising:	1. **Light-emitting diode** comprising
1.1 a light emitting structure	1.1. a light emitting structure;
1.2 mesa-etched areas (150)	1.2 mesa-etched areas (150);
1.3 a reflective electrode (140)	1.3 a reflective electrode (140);
1.4 a lower insulation layer (200)	1.4 a lower insulation layer (200);
1.5 a current spreading layer (210)	1.5 a current spreading layer (210);
1.6 an upper insulation layer (220)	1.6 an upper insulation layer (220);
1.7 a first pad (230)	1.7. a first pad (230);
1.8 a second pad (240)	1.8 a second pad (240).
2. the **light-emitting structure**	2. The **light-emitting structure**
2.1 is formed on a substrate (100)	2.1. is formed on a substrate (100);
2.2 comprising	2.2. comprising:
2.1.1 a first conductivity type semiconductor layer (110),	2.1.1. a semiconductor layer (110) of a first conductivity type,
2.1.2 an active layer (120) and	2.1.2. an active layer (120) and
2.1.3 a second conductivity type semiconductor layer (130);	2.1.3. a semiconductor layer (130) of a second conductivity type.
3. **mesa-etched areas** (150) formed from the surface of the second conductivity type semiconductor layer (130) to the first conductivity type semiconductor layer (110);	3. The **mesa-etched areas** (150) are formed from the surface of the second conductivity type semiconductor layer (130) to the first conductivity type semiconductor layer (110) of the first conductivity type.

4. **the reflective electrode** (140)	4. The **reflective electrode** (140)
4.1 is formed on the second conductivity type semiconductor layer (130)	4.1 is formed on the semiconductor layer (130) of the second conductivity type;
4.2 includes	4.2. has:
4.2.1 a reflective metal layer (142),	4.2.1. a reflective metal layer (142);
4.2.2 a barrier metal layer (144)	4.2.2. a barrier metal layer (144);
4.2.3 a stress relieving layer (143)	4.2.3. a stress relieving layer (143);
4.2.3.1 the stress relieving layer (143)	4.2.3.1. The stress relieving layer (143)
4.2.3.1.1. is formed between the reflective metal layer (142) and the barrier metal layer (144),	4.2.3.1.1. is formed between the reflective metal layer (142) and the barrier metal layer (144) formed;
4.2.3.1.2. has a coefficient of thermal expansion between the coefficient of thermal expansion of the reflective metal layer (142) and the coefficient of thermal expansion of the barrier metal layer (144);	4.2.3.1.2. has a coefficient of thermal expansion between the coefficient of thermal expansion of the reflective metal layer (142) and the coefficient of thermal expansion of the metal barrier layer (144).
5. **the lower insulation layer** (200)	5. The **lower insulation layer** (200)
5.1 covers an overall surface of the structure formed by	5.1 covers the entire surface of the structure formed by:
5.1.1 the first conductivity type semiconductor layer (110),	5.1.1. the semiconductor layer (110) of the first conductivity type,
5.1.2. the active layer (120),	5.1.2. the active layer (120),
5.1.3 the second conductivity type semiconductor layer (130),	5.1.3. the semiconductor layer (130) of the second conductivity type;
5.1.4 the mesa-etched areas (150)	5.1.4. the mesa-etched areas (150) and
5.1.5 and the reflective electrode (140),	5.1.5. the reflective electrode (140).
5.2 allowing an upper surface of the reflective electrode (140) to be partially exposed therethrough, further having openings disposed near an edge of the substrate, which allow the surface of the first conductivity type semiconductor layer (110) to be exposed therethrough in the mesa-etched areas (150);	5.2. allows an upper surface of the reflective electrode (140) to be partially exposed therethrough; and further has openings disposed near an edge of the substrate, which allow the surface of the first conductivity type semiconductor layer (110) to be exposed therethrough in the mesa-etched areas (150);
6**. the current spreading layer (210)**	6. The **current spreading layer** (210)
6.1 formed on the lower insulation layer (200)	6.1. is formed on the lower insulation layer (200) formed on the lower insulation layer (200);
6.2 covering the first conductivity type semiconductor layer (110)	6.2. covers the semiconductor layer (110) of the first conductivity type;
6.3 and being electrically connected to the first conductivity type semiconductor layer (110);	6.3. is electrically connected to the semiconductor layer (110) of the first conductivity type.
7. the **upper insulation layer** (220)	7. The **upper insulation layer** (220)
7.1 formed on the current spreading layer (210),	7. is formed on the current spreading layer (210) formed on the current spreading layer (210).
7.2 with both the current spreading layer (210) and the reflective electrode (140) being partially exposed through the upper insulation layer (220);	7.2. both the current spreading layer (210) and the reflective electrode (140) are partially exposed through the upper insulation layer (220) .

8. the **first pad** (230) electrically connected to the current spreading layer (210) exposed through the upper insulation layer (220); and	8. The **first pad** (230) is electrically connected to the current spreading layer (210), which is exposed through the upper insulation layer (220).
9. the **second pad** (240) electrically connected to the reflective electrode (140) exposed through the upper insulation layer (220).	9. The **second pad** (240) is electrically connected to the reflective electrode (140) exposed through the upper insulation layer (220). exposed through the upper insulation layer (220).

31. The principles applicable to the interpretation of claims were set out in this Court's order in Case UPC_CoA_335/2023 (NanoString v 10x Genomics, headnote 2, corrected). The patent claim is not only the starting point, but also the decisive basis for determining the scope of protection of a European patent under Article 69 EPC in conjunction with the Protocol on the Interpretation of Article 69 EPC. The interpretation of a patent claim does not depend solely on its exact wording in the linguistic sense. Rather, the description and drawings must always be consulted as aids to interpreting the patent claim and not only to resolve any ambiguities in the patent claim.

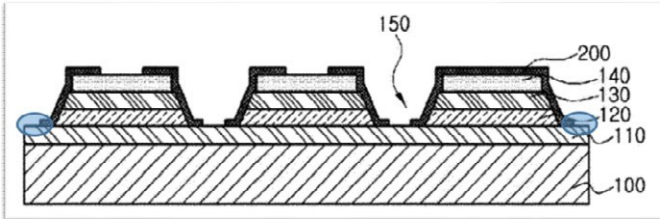
The subject matter of the invention

32. In flip-chip type LEDs, the contact electrodes of the first and second semiconductor layers are each located on the back of the chip, while light is emitted from the LED on the opposite side of the chip. The first electrical contact point is located in the mesa-etched areas (i.e. outside the mesa), where the current expansion layer is electrically connected to the exposed first semiconductor layer. The second contact point is the reflective electrode located on the mesa. The current supplied to the first pad connected to the current expansion layer causes a lateral current flow in the first semiconductor layer from the exposed areas of the first semiconductor layer in the mesa-etched areas through the active layer in the respective mesa where light generation takes place and through the second semiconductor layer to the reflective electrode connected to the second pad. This lateral current flow causes problems with the uniform distribution of electrical current across the entire surface of the active layer, i.e. the lateral extension of the mesa. This is because light emission is proportional to the current flow in the active layer, which in turn can vary depending on the path taken by the current due to the ohmic resistance of the various conductive components of the LED. Uneven current distribution leads to uneven light emission, reduced efficiency, local overheating and a shortened LED lifetime.
33. The aim of the invention is to improve the current spread and light output of (in particular flip-chip) LEDs. A further aim of the invention is to reduce thermally induced mechanical stresses in the electrode.

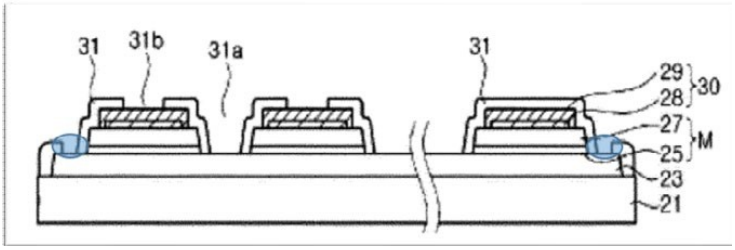
*Fe*ature *5.2* – "Openings [...] arranged near an edge of the substrate"

34. For the present method, the design of the "openings [...] arranged near an edge of the substrate" mentioned in feature 5.2 is of particular importance.
35. Feature 5 requires that the lower insulating layer (200) cover the entire structure formed by the first semiconductor layer (110), the active layer (120), the second semiconductor layer (130), the meso-etched areas (150) and the reflective electrode (140). Openings in the lower insulating layer allow an upper surface of the reflective electrode to be partially exposed through them. Further openings allow the surface of the first semiconductor layer (110) to be exposed through them in the mesage-etched areas (150). Feature 5.2 requires that these latter openings be located near an edge of the substrate.

36. The "openings near an edge of the substrate" required in feature 5.2 can be found in the patent specification in relation to Figures 6 and 7. With reference to Figure 6, paragraph [0075] states:
"After the plurality of mesas M are formed, an edge of the first conductive semiconductor layer 23 can also be etched. As a result, the upper surface of the substrate 21 can be exposed."
37. As can be seen from the annotated sectional view of Figure 19, which is similar in this respect (in Figure 6, the plurality of mesas M are arranged in an island-like manner and surrounded by mesa-etched areas; Figure 19, on the other hand, has strip-shaped mesa-etched areas, also at the edge of the substrate, with the mesas in between), this leads to exposure of the first semiconductor layer 23 (110 in Figure 19) at the edge of the substrate (indicated by blue markings).



38. With reference to Figure 7 and the description in paragraphs [0077] and [0078], it states:
"With reference to Figure 7, a lower insulating layer 31 is formed, covering the majority of the mesas M and the semiconductor layer 23 of a first conductivity type. The lower insulating layer 31 has openings 31a, 31b that enable electrical connection in certain areas with the semiconductor layer 23 of a first conductivity type and the semiconductor layer 27 of a second conductivity type. The lower insulating layer 31 has, for example, openings 31a through which the semiconductor layer 23 of a first conductivity type is exposed, and openings 31b through which the reflective electrodes 30 are exposed.
The openings 31a are arranged in a region between the mesas M and near an edge of the substrate 21 and may have an elongated shape extending along the mesas M. The openings 31b, on the other hand, are arranged only on the mesas M so as to be biased towards the same ends of the mesas.
39. As can be seen from the annotated Figure 7, the openings (marked in blue) are located near the edge of the substrate, with an insulating layer between the openings 31a and the edge of the substrate itself.



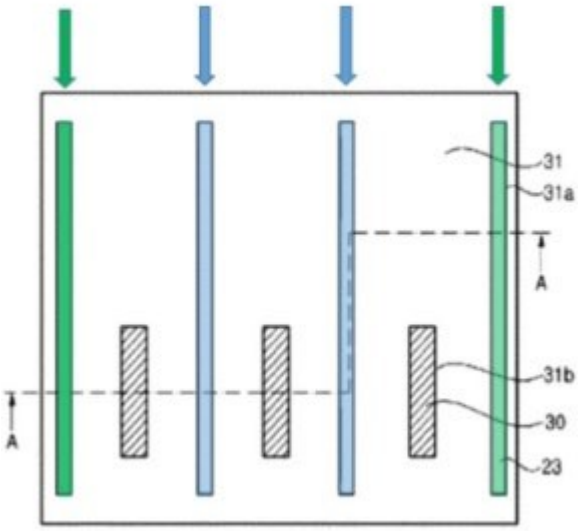
40. With regard to both Figure 6 and Figure 7, the specification clearly states that the openings or etched mesa areas are located both between two mesas and between the mesa and the edge of the substrate.

Purpose and effect of feature 5.2

41. expert klein has explained that the contact between the first semiconductor layer and the current expansion layer near the edge of the substrate required in feature 5.2 is intended to improve current distribution in LEDs. This is achieved by shortening the path that the

current has to travel in the first semiconductor layer 110 is shortened, thereby reducing electrical resistance and achieving a more uniform current distribution across this layer.

42. Viosys essentially agrees with this. It was stated (in the statement of defence in the nullity action (KE) Rn. 31–
32) that one finding of the invention is that current distribution can be improved by exposing end areas of the n-semiconductor layer outside the mesa at the edge of the substrate in mesage-etched areas. In these areas, the current can be distributed via the current expansion layer with low electrical resistance from any point on the mesa surface. According to Viosys, in order to achieve the most homogeneous current distribution possible within the semiconductor material, the distance that the current must travel from any point in the area covered by the mesa to the nearest contact point of the n-layer should be as short as possible.
43. This can be illustrated by the annotated Figure 7 (created by Viosys, KE Rn. 34), which shows the openings in mesa-etched areas between the mesas in blue and in mesa-etched areas near the substrate edge in green. Without the openings in the green mesa-etched areas, the middle mesa would be supplied with current from both sides, while the mesas on the outside of the LED chip would only be supplied with current from one side. Due to the longer distance that the current has to travel to the outer ends of these mesas, the light emission would not be homogeneous.



44. The LKD further found that feature 5.2 serves the purpose of improving current spreading. This is achieved by shortening the current path in the first semiconductor layer, thereby reducing electrical resistance and increasing the efficiency of the LED (contested decision, page 26, paragraph cc) (2).
45. The Court of Appeal concurs with this view.

Interpretation of feature 5.2

46. The Court of Appeal agrees with expert Klein that, in view of the objective of improved current distribution, the skilled person would understand feature 5.2, in particular 'openings near an edge of the substrate', to mean that, in the case of multiple mesas, the openings are arranged in such a way that the current flows into the mesa not only from the mesa-etched areas located between the mesas, but also from the mesa-etched areas at or near the edge of the substrate. Thus, current flows from the mesa-etched areas located outside the mesa into each mesa *from both sides*, regardless of whether the mesa is located in the centre or on the outside of the LED chip.

This keeps the current path as short and as uniform as possible. This means that there is no further mesa (area) between the outer openings and the edge of the substrate, as this mesa (area) would then not receive current from both sides.

47. Viosys agreed with this in the first instance. It stated (KE para. 36) that, based on these technical aspects of current distribution in an LED according to the invention, the skilled person would understand the combination of features [5.2] and [6.3] in the sense that "in order to achieve the desired current distribution, the n-layer is contacted in an exposed area in the peripheral edge outside the area of the chip surface occupied by the active area, i.e. by the mesa(s)" (emphasis added).
48. That this was Viosys' understanding of feature 5.2 can also be inferred from its response to an attack on inventive step by expert klein based on D3 (US 2005/0067624) as a reasonable starting point. The embodiment of Figures 5 (shown below), 6 and 7 of this document (referred to by the parties as the first embodiment) shows hole-like, mesa-etched areas (similar to the embodiment of Figures 24 to 26 of the patent).

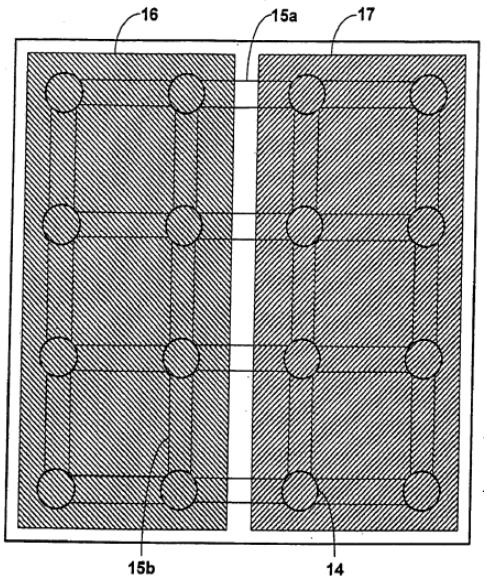


Fig. 5

49. Viosys has argued that this first embodiment of D3 does not disclose feature 5.2. In this context, Viosys has stated the following (KE, paras. 46–47):
"Feature [5.2] is not disclosed in D3 in connection with the first embodiment. The n-layer is not exposed near the edge of the substrate. This can be seen from the illustration in Figure 6 of D3. There, it can be seen where the n-layer 11 is contacted on its upper side by the metal fillings 21 connected to the struts 15a (marked with coloured circles in the drawing):

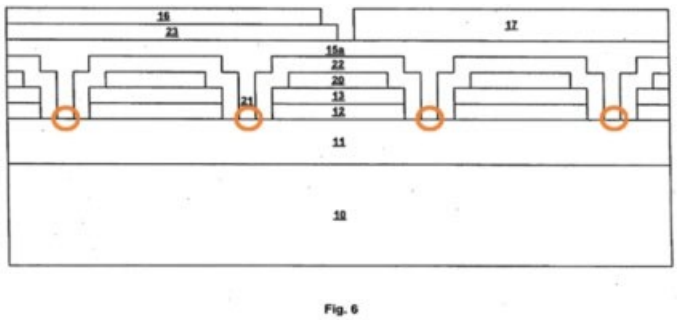


Fig. 6

The contact points are not located near the edge of the substrate 10, not even the two outer contact points. The n-layer extends beyond the outer contact points towards the edge

of the substrate with the outer mesa areas lying above it. In the first embodiment of D3, the n-layer is therefore contacted exclusively within the area of the n-layer occupied by the mesa and not in an area exposed at the edge, i.e. at the outer circumference of the n-layer in the periphery of the mesa area, as required by feature [5.2] (in combination with feature [6.3]). This is therefore not realised in the first embodiment of D3."

50. In the appeal proceedings, Viosys changed its position and stated (BE para. 25) that the LKD had rightly decided that these openings must be located near the edge. It is not necessary for these openings to be located outside the mesa. As can be seen from the above, the Court of Appeal does not agree with either the LKD or Viosys on this point.
51. The purpose and effect of feature 5.2 (see above, paragraphs 41-44), as directly apparent from Figures 6 and 7 and the description discussing those figures (see above, paragraphs 34-40), will lead the skilled person to understand that there should be no further mesa (area) between the outer opening and the edge of the substrate. The fact that Figures 24-26 only show openings within the mesa area does not lead the skilled person to any other conclusion. The skilled person will assume that this embodiment is not covered by claim 1. This idea is reinforced by two facts: on the one hand, the description does not discuss feature 5.2 in relation to Figures 24 to 26 at all, and on the other hand, the patent also contains Figures 27 to 36, which, as the parties agree, have nothing to do with the invention according to Claim 1.

Other features

52. The parties disagree on the interpretation of other features of claim 1, such as the "current expansion layer" of feature 6. However, since these features are not decisive for the outcome of the present proceedings, the Court of Appeal disregards them.

Inadmissible extension

53. The Court of Appeal first examines the alleged invalidity of the patent due to an inadmissible extension of its subject matter.
54. expert klein asserts that the parent application does not disclose a single mesa. However, if the embodiment of Figures 24 to 26 is considered to be a disclosure of a single mesa, feature 5.2 is not disclosed in this embodiment.

Scope of the appeal

55. The parties agree that claim 1 also covers embodiments (LEDs) that comprise only one mesa. This was also the opinion of the LKD, which the Court of Appeal concurs with.
56. In the counterclaim for revocation (WNE), para. 18, expert klein expressly stated that, in its opinion, the subject matter of claim 1 goes beyond the content of the original application, as it also covers embodiments with a single mesa (WNE para. 21 with reference to the parent application filed as Annex B5 and WNE para. 23 with reference to Figures 2–11 and 13–26).
57. Viosys countered this argument by stating that Figures 24 to 26 show a further embodiment (which differs from those shown in Figures 2-11 and 13-23) and disclose the presence of only a single mesa on the LED chip (KE para. 5).
58. This view was expressly disputed by expert klein in its reply (para. 2), which states: "However, the defendant in the nullity proceedings is of the opinion that such a disclosure of an LED with the

features of claim 1 and a mesa can be derived from Figures 24 to 26. This view is incorrect." expert klein then goes on to argue that feature 5.2 is not disclosed in the embodiment of Figures 24-26 and concludes in para. 14: "Insofar as [...] claim 1 comprises a design with a mesa in which, according to feature [5.2], contacting takes place near the edge of the substrate, this is not disclosed in the original application documents" (emphasis added).

59. The argument by expert klein that feature 5.2 is not disclosed must therefore be understood as a subordinate argument. This means that if Figures 24 to 26 do indeed disclose a single mesa, it is further argued that feature 5.2 is not disclosed therein. Viosys therefore wrongly claimed (reply, para. 1) that expert klein had conceded that the parent application also disclosed an LED with only one mesa in conjunction with the embodiment shown in Figures 24 to 26.
60. In para. 4 of its appeal statement (BB), expert klein contests the contested decision in its entirety. In BB para. 12, expert klein states: "The inadmissible extension already results from the fact that patent claim 1 covers both embodiments with only one mesa and with a plurality of mesas. A disclosure relating to a single mesa is only apparent from the fourth embodiment according to Figures 24 to 26. However, this embodiment according to Figures 24 to 26 does not have the further, additional features of claim 1 and does not disclose these features." Even though expert klein could admittedly have expressed itself more clearly here, the Court of Appeal is of the opinion that, in view of expert klein's submission in the first instance, it can be assumed that expert klein maintained both arguments: Firstly, that an embodiment with a single mesa is not disclosed in the parent application, and secondly, that if the embodiment of Figures 24 to 26 discloses a single mesa, feature 5.2 is not disclosed therein. This was confirmed by expert klein in the oral proceedings and Viosys responded accordingly. Viosys was familiar with the argument that a single mesa is not disclosed in Figures 24-26, as expert klein had put forward the same argument in relation to EP 320, which is the subject of parallel nullity and infringement proceedings. The oral proceedings in those proceedings had taken place the day before.
61. In view of this, Viosys wrongly claimed (appeal response (BE) para. 49) that expert klein had conceded (abandoning its first-instance submission) that a embodiment with a mesa was disclosed in Figure 24 of the parent application.
62. With reference to R.222.2 RPC, Viosys objected to expert klein's arguments in the appeal proceedings that features 5.2 and 4.2 were not disclosed (BE para. 49). With regard to the alleged non-disclosure of feature 5.2, it follows from the above that expert klein had already expressly raised this point in the first instance proceedings, so that there is no reason to disregard this argument.
63. In view of the findings of the Court of Appeal regarding the non-disclosure of feature 5.2, which are set out below, it is not necessary to decide whether the argument that features 4.2.2 and 4.2.3 are not disclosed in relation to Figures 24 to 26 was raised for the first time in the appeal by expert klein.

Principles

64. An inadmissible extension of the subject matter occurs when the subject matter of the granted claim extends beyond the content of the application as originally filed. In order to determine this, the court must first ascertain what information the skilled person, based on an objective assessment and with reference to the filing date, would immediately and unambiguously derive from the entirety of the application as filed, using his general technical knowledge. In doing so,

implicitly disclosed subject matter must also be regarded as part of the content, i.e. subject matter that clearly and unambiguously results from what is expressly stated.

65. If, as in this case, the patent has been derived from a divisional application, this requirement applies to each earlier application. The subject matter of the granted claim 1 must therefore not go beyond (1) the disclosure of the originally filed application for the contested patent and (2) the disclosure of the original PCT application which entered the regional phase and constitutes the parent application of the divisional application.

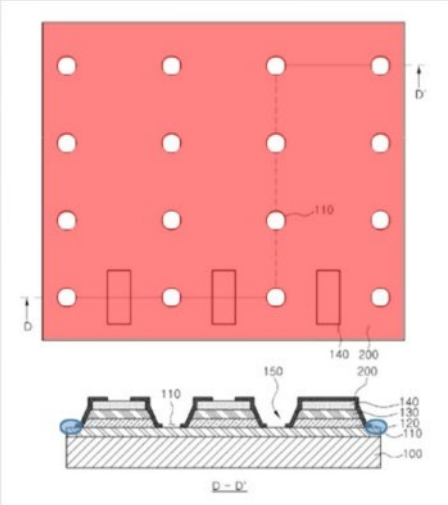
Relevance of the disclosure of a single mesa

66. expert klein argued that an embodiment disclosing only a single mesa had not been disclosed in the parent application. It referred to several paragraphs in the parent application which refer (only) to LEDs with more than one mesa, such as on page 3 under the heading "Technical solution" and on page 6 under the heading "Advantageous effects". expert klein also argued (WNE paras. 27-29) that the problem which the patent purports to solve arises precisely because there are several mesas and the proposed composition of the LED, according to claim 1, is only necessary for embodiments with several mesas.
67. The LKD found that, insofar as [expert klein] attempts to justify an inadmissible extension on the grounds that the original patent application disclosed only designs with several mesas, but not those with one mesa, the mesas themselves are not mentioned in patent claim 1. Rather, the presence of mesa-etched areas is sufficient, but also necessary (contested decision, page 28, paragraph 2 a)).
68. The Court of Appeal does not share the LKD's view that claim 1 does not contain an extension, even if the parent application only disclosed embodiments with multiple mesas, since it does not expressly mention "a mesa". It should be remembered that claim 1 is a device claim protecting an LED with multiple features. One of these features is feature 1.2: mesa-etched areas (150). It is common knowledge that the skilled person recognises that mesa-etched areas form one or more mesas. Viosys itself has argued that, in the context of LED technology, a person skilled in the art understands a mesa to be a structure or topography in the form of a raised surface or plateau on the surface of a semiconductor material, which is formed by etching (KE, para. (6); underlining added).
69. Viosys argued that a plurality of mesas could not be an essential feature of the originally disclosed invention, since the problem of current distribution in LEDs with a large surface area exists regardless of the number of mesas on the LED chip. The Court of Appeal rejects this argument.
70. Claim 1 of the parent application expressly refers only to an LED with a plurality of mesas. Furthermore, on page 3, under the heading "Technical Solution," the parent application describes that, according to one aspect of the invention, an LED comprises a plurality of mesas, reflective electrodes each disposed on the corresponding mesa area, and a current spreading layer covering the plurality of mesas and the semiconductor layer of the first conductivity type. It is then mentioned that the LED has improved current spreading due to the current spreading layer because (emphasis added) the current spreading layer covers the plurality of mesas and the first semiconductor layer. As expert klein rightly pointed out, this underlines that claim 1 claims to solve the technical problems arising from the presence of a plurality of mesas. Therefore, the number of mesas cannot be considered irrelevant.

71. Insofar as Viosys sought to argue that the core of the invention lies in the composition of the reflective electrode according to feature 4 and that the number of mesas is irrelevant, this must also be rejected. The parent application merely describes the composition of each of the reflective electrodes (from page 3, last paragraph, to page 4, second paragraph). This description is now reflected in feature 4 of claim 1 as a further (possible) element of the described LED of the invention. Even if the composition of the electrodes can contribute to solving the problem of providing an LED with improved current spread and the number of mesas is not relevant for this, the composition of the electrode(s) as prescribed in feature 4 is only one element of the invention, alongside other elements of the LED according to claim 1 that also contribute to the solution, such as feature 5.2. As expert klein has rightly pointed out, feature 5.2 cannot be interpreted away by Viosys focusing exclusively on feature 4.
72. Since it is undisputed that claim 1 covers LEDs with only one mesa, it follows that claim 1 covers an additional subject matter if embodiments (LEDs) with only one mesa are not disclosed in the parent application.
73. Viosys argues that the parent application discloses embodiments with a single mesa in Figures 24 to 26 and that such single-mesa embodiments result from the cutting method described on page 12 of the parent application. As explained below, both arguments are unsuccessful.

Disclosure of a single mesa in the embodiment shown in Figures 24 to 26?

74. Viosys concedes that the embodiments of Figures 2 to 11 and Figures 13 to 23 disclose LEDs with multiple mesas. However, it claims that a single mesa is part of the disclosure of the parent application because the further embodiment of Figures 24 to 26 contains only a single mesa. The LED chip shown in Figures 24 to 26 has only a single plateau, a uniformly raised area. Several hole-shaped mesa-etched areas were etched into this plateau in a rectangular pattern, as described on page 22, paragraph 6 of the parent application. In Viosys's view, the red area in Figure 24, commented on below, therefore shows the single mesa:



75. The Court of Appeal considers that this is not the understanding of a person skilled in the art when viewing these figures and reading the parent application in its entirety. A person skilled in the art will understand from the parent application that there will be one mesa for each electrode. This is apparent from page 3 (Annex B5), where it states under the heading "Technical solution" that an LED according to one

aspect of the invention comprises reflective electrodes, each arranged on the corresponding mesa area (underlining added).

76. Page 22 of the parent application states that Figures 24 to 26 are top views and sectional views of a light-emitting diode module with the structure of Figure 12 according to a further embodiment of the invention. The application mentions that in Figure 24, a lower figure is a sectional view along line D-D' of the top view of Figure 24, wherein line D-D' is interrupted along a dashed line and shows only a continuous line section. This is followed by an explanation that in some areas the reflective electrodes 140 are exposed, in the message-etched areas 150 the first semiconductor layer 110 is exposed, and furthermore, in an area where the reflective electrodes 140 are not exposed, the lower insulating layer 200 completely shields the reflective electrodes 140. The paragraph spanning pages 22 and 23 mentions that, in the sectional view along line D-D', two reflective electrodes 140 are exposed in an area that intersects the two exposed reflective electrodes 140 (underlining added).
77. Looking at Figures 24 to 26 with this description in mind, the skilled person will recognise that the embodiment of Figures 24 to 26 has multiple electrodes. Based on the application, which describes both exposed and covered reflective electrodes, the skilled person will understand, in combination with the cross-sectional view in Fig. 24, that this cross-sectional view shows two exposed electrodes and a third electrode that is completely covered by the insulating layer 200. Since the number of electrodes indicates the number of mesas, the skilled person will recognise that the embodiment of Figures 24 to 26 has multiple – three – mesas.
78. This understanding is confirmed by the similarity of the sectional view in Figure 24 compared to the sectional views in Figures 9, 10, 19, 20, 21 and 23 (Figures 9, 20, 21 and 23 are not shown here, but are similar in this respect to the sectional views in Figures 10 and 19). It is undisputed that these figures show three mesas. Since there is no indication in the patent specification that the sectional view of Fig. 24 shows only one mesa despite the similarity, the skilled person would understand this figure to also show the presence of three mesas.

Disclosure of a single mesa as a result of the cutting process?

79. As a second line of argument that the parent application also discloses embodiments with only one mesa, Viosys refers to page 12, paragraph 5 of the parent application and claims that in the embodiment of Figure 10, several strip-shaped mesas are initially provided and that, according to the description, after the pads 37a and 37b have been applied, the chip is split between the mesas and divided into several individual LEDs. This ultimately results in LEDs with only one mesa.
80. The relevant paragraph reads: "The substrate 21 is then divided into individual light-emitting diode chips, resulting in the final light-emitting diodes."
81. Contrary to what Viosys claims, this paragraph does not state that "the chip is split between the mesas". The parent application does not provide any indication of how the cutting process is carried out, let alone that it is carried out in such a way that the resulting individual LEDs each consist of only one mesa. On the contrary, the immediately following paragraphs describe a single LED (diode in the singular) comprising "the mesas M" or "the plurality of mesas M" or "each of the mesas M". The skilled person will therefore understand that the cutting process results in individual LEDs, each containing more than one mesa.
82. The Court of Appeal could find no reference anywhere in the parent application to an LED with only one mesa that could support Viosys's view that the cutting process would result in an LED with one mesa. In the absence of any clear indication to this effect in the parent application and a substantiation by Viosys – for example by an

Party expert opinion – which shows that the skilled person inevitably assumes that the cutting process results in an LED with a single mesa, the mere theoretical possibility that an LED with a single mesa could be produced is not sufficient to constitute a clear and unambiguous disclosure.

83. For the sake of completeness, the Court of Appeal also points out that Fig. 12 cannot be considered to disclose an embodiment with a single mesa, as the parent application clearly states that it is only a *partial view* (see pages 7 and 14 (paragraph 5) of the parent application).

Conclusion on the disclosure of a single mesa

84. Based on the above, the Board of Appeal considers that claim 1 contains an inadmissible extension of the subject matter, as it covers embodiments with a mesa that are not clearly and unambiguously disclosed in the parent application. For this reason alone, the contested decision of the LKD cannot be upheld.

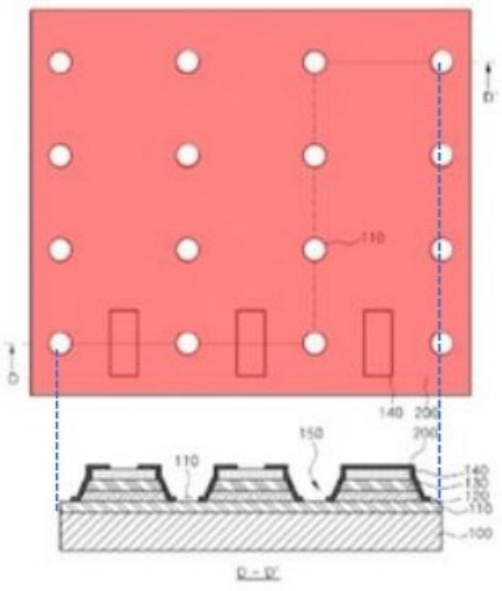
Disclosure of feature 5.2 – "openings near the edge of the substrate" – in the embodiment of Figures 24 to 26?

85. The Court of Appeal also agrees with expert klein's argument that even if the embodiment of Figures 24 to 26 disclosed a single mesa, and was therefore the only embodiment that could serve as the basis for Claim 1, it did not disclose feature 5.2.
86. With regard to the embodiment of Figures 24 to 26, the parent application states the following on page 22, paragraphs 5 and 6:
    "Figures 24 to 26 show top views and sectional views of a light-emitting diode module with the structure shown in Figure 12 according to a further embodiment of the invention.
    With reference to Figure 24, in this embodiment, the mesage-etched areas 150 from Figure 18 are formed in a hole-like manner. Accordingly, a first semiconductor layer 110 is exposed in a substantially circular shape" (underlining added).
87. The reference to Figure 18 is understood by those skilled in the art here as a cross-reference to the paragraph that spans pages 16 and 17. This paragraph describes the etching process in relation to the embodiments of Figures 13–18. It also mentions that the meso-etched areas may be strip-like or hole-like.
    "With reference to Figure 14, a portion of the active layer 120 and a portion of the second semiconductor layer 130 are removed by a conventional etching process. As a result, the first semiconductor layer 110 is partially exposed. The etching process exposes the upper surface of the first semiconductor layer 110 and the side surfaces of the active layer 120 and the second semiconductor layer 130. As a result, the active layer 120 and the second semiconductor layer 130 are partially removed to form trenches and holes through the etching process. In other words, the mesage-etched areas 150 formed from the surface of the second semiconductor layer 130 in Figure 13 to the surface of the first semiconductor layer 110 may be trench-like, strip-like or hole-like.
88. With reference to Figure 18, this is repeated on page 19, paragraph 4: "*As described above, the mesage-etched areas 150 may be strip-like or hole-like.*"
89. The parent application then describes the embodiments of Figures 19 to 23 and 24 to 26, which show examples of strip-like and hole-like mesage-etched areas, respectively, as can be seen from the references to Figure 18 in each case. Page 20, paragraphs 1 and 2 state:

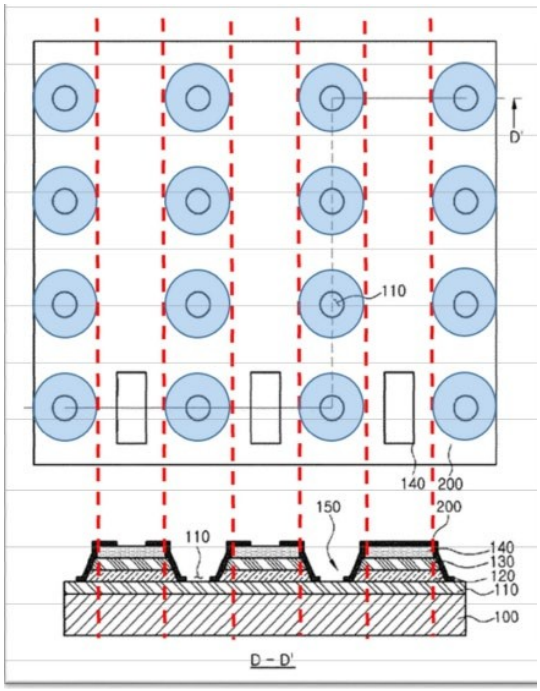
"Figures 19 to 23 are top views and sectional views of a method for manufacturing the light-emitting diode with the structure shown in Figure 12 according to another embodiment of the present invention. With regard to Figure 19, it is assumed that the mesage-etched areas 150 from Figure 18 are strip-shaped. (...)" (underlining added).

A similar statement is made for Figures 24-26, as quoted above in paragraph 86.

90. Viosys's assertion that the parent application discloses a further embodiment corresponding to Figures 12 to 23, which is not shown in the figures and in which the meso-etched areas are hole-shaped, as an alternative to the strip shape shown in the figures, does not correspond to the understanding of the skilled person, who will recognise that this alternative is in fact shown in Figures 24 to 26. Thus, it cannot be accepted that the parent application also discloses, in connection with the embodiment of Figures 12 to 23, a variant with only a single uninterrupted mesa (with hole-shaped mesa-etched areas), wherein the first semiconductor layer (110) according to Figure 19 is exposed at the edge through the lower insulating layer (200) at the edge in the sense of feature 5.2, as claimed by Viosys (reply, para. 7).
91. The embodiment of Figures 24 to 26 is described on pages 22 and 23 of the parent application. Neither are openings/mesa-etched areas at or near the edge of the substrate mentioned, nor are they clearly and unambiguously derivable from the parent application.
92. If the embodiment according to Figures 24 to 26 discloses a single mesa, then there is clearly a mesa area towards the edge of the substrate beyond the outer openings. As a result, the outer contact points between the current expansion layer and the first semiconductor layer are located *within* the mesa area and not outside the mesa and near the edge of the substrate, without there being another mesa (area) as required in feature 5.2.
93. The cross-sectional view shown below in Figure 24 – which, as Viosys noted, is virtually identical to the cross-sectional view shown in Figure 19, which indisputably shows openings near an edge of the substrate – does not lead to a different assessment.
94. As expert Klein correctly noted, this cross-sectional view does not show a cut from the first arrow D to the other arrow D, but rather a cross-section from approximately the centre of the outer, meso-etched area on the left side to approximately the centre of the outer, meso-etched area on the right side, without showing the meso-etched area extending between these meso-etched areas and the edge of the substrate on the left and right sides, respectively. This is evident from the drawing shown below, which is annotated by expert klein.



95. Even though Viosys stated in its statement of defence that the red-coloured area in the annotated Figure 24 shown above in para. 74 (and para. 94), Viosys argued in its rejoinder that this red-coloured area does not show the area covered by the mesa, but rather the lower insulating layer covering it, and that the geometry of the mesa and the mesa-etched areas cannot be deduced from it. The openings shown are the openings in the lower insulating layer 200 in which, according to feature 5.2, the first semiconductor layer is exposed. The hole-shaped mesa-etched areas have a significantly larger diameter, so that the outer mesa-etched areas extend to the outermost edge of the substrate 100. Further out towards the edge, there is therefore no space left for mesa areas, just as in the case of the embodiment in Figure 19, as shown in the annotated Figure 24 below. This is the argument put forward by Viosys (Duplik Rn. 12–14).



96. This argument must be rejected. Expert Klein has rightly pointed out that there is no reference to this interpretation of Figure 24 in the parent application. On the contrary, it explicitly states: *"Furthermore, in Figure 24, the hole-like mesa-etched areas 150 are exaggerated for the sake of simplicity. Therefore, the number and shape of the hole-like mesa-etched areas 150 may vary depending on the design."* The skilled person therefore does not know exactly what size the mesa-etched holes are, but would rather expect them to be smaller than shown and certainly not as large as suggested by Viosys. This would also be contrary to the purpose of the invention. As Viosys itself has emphasised (para. 24 BE), light generation takes place exclusively in the active layer. In order to maximise light emission, it is generally an objective to keep the proportion of mesa-etched areas (in which the active layer is missing) on the total chip surface as small as possible. The area occupied by the mesa, on the other hand, should be as large as possible.
97. Expert Klein also pointed out that a person skilled in the art would not expect the diode to be manufactured in this way, because if the outer openings actually extended to the very edge of the substrate, this would result in the edge of the substrate having a very fragile and breakable serrated side. According to expert klein, there must therefore be at least some material beyond the outer openings to prevent breakage. Viosys did not convincingly dispute this.

98. Viosys's appeal argument that Figure 24 discloses feature 5.2 because it is sufficient for openings to be located near the edge, even if they are arranged within the mesa area, must be rejected. This is based on an incorrect interpretation of feature 5.2. This feature requires that there be no further mesa (area) between the outer openings and the outermost edge of the substrate and is therefore not disclosed by openings located *within* the mesa area.

Conclusion on the disclosure of feature 5.2

99. Based on the above, the Board of Appeal considers that claim 1 contains an inadmissible extension of the subject matter, since – if an embodiment with a single mesa were disclosed in the embodiments of Figures 24 to 26 of the parent application – feature 5.2 would not be clearly and unambiguously disclosed therein. For this reason alone, the contested decision of the LKD cannot be upheld.

Conclusion on the inadmissible extension

100. In view of the above, the Court of Appeal considers that claim 1 is invalid due to extension of the subject matter. Claims 4, 5, 6 and 9 depend on claim 1 and are also invalid for the same reasons.

Subordinate requests

101. The auxiliary requests all relate to embodiments with a single mesa and therefore cannot lead to a valid claim. It is therefore not necessary to discuss them.

Further grounds for invalidity

102. The further grounds for invalidity put forward by expert klein do not need to be discussed.

Infringement action

103. In view of the invalidity of the patent, there is no need to decide on the alleged infringement of the patent by the contested embodiment.

Cost

104. Viosys is to be regarded as the unsuccessful party in the appeal proceedings. It is ordered to pay expert's costs for the appeal proceedings and the first instance proceedings, both for the counterclaim for revocation and for the infringement action.

DECISION

In the counterclaim for revocation

The Court of Appeal

- lifts the contested decision in its entirety;
- declares claims 1, 4, 5, 6 and 9 of the contested patent invalid with effect for the territories (Austria, Belgium, Germany, France, Italy, Luxembourg, the Netherlands and Sweden);
- orders Viosys to pay the costs of the proceedings both on appeal and at first instance.

In the infringement action

The Court of Appeal:

- sets aside the contested decision in its entirety;
- dismisses all of Viosys' claims;
- orders Viosys to pay the costs of the proceedings both on appeal and at first instance.

Issued on 2 October 2025

Rian Kalden Date: 2025.10.02 08:27:16 +02'00

Rian Kalden, Presiding Judge and Rapporteur

Patricia Ursula Rombach Digitally signed by Patricia Ursula Rombach Date: 2025.10.02 08:05:29 +02'00

Patricia Rombach, legally qualified judge

Digitally signed by Åsa Ingeborg Simonsson Date: 2025.10.02 06:34:29

Ingeborg Simonsson, legally qualified judge

TORSTEN DUHME Digital signed by TORSTEN DUHME Date: 2025.10.02 09:45:26

Torsten Duhme, technically qualified judge

Max Wilhelm Tilmann Digitally signed by Max Wilhelm Tilmann Date: 02.10.2025 08:36:55

Max Tilmann, technically qualified judge