Unified Patent Court
Einheitliches Patentgericht
Juridiction unifiée du brevet

**Hamburg - Local Chamber**

# UPC_CFI_58/2024

# Decision

# of the Court of First Instance of the Unified Patent Court Hamburg Local Division

# issued on 19 February 2025

GUIDING PRINCIPLES

1. For the interpretation of a patent whose purpose to overcome the time delay, the so-called latency time, in the processing of data packets and in particular headers during transmission in a wireless network.
2. When interpreting the patent claim, the application description and express disclosures in the description of the patent specification must be taken into account in addition to the wording.

KEYWORDS

Art. 69 EPC, Art. 25 UPCA

PLAINTIFF

| | | |
|---|---|---|
| | **Lionra Technologies Ltd.**<br>(Applicant) - The Hyde Building, Suite 23, The Park - 00000 - Carrickmines, Dublin 18, Ireland - IE | Represented by: Dr Thomas Adam |

DEFENDANT

| | | |
|---|---|---|
| 1) | **Cisco Systems GmbH**<br>(Defendant) - Parkring 20 - 85748 - Garching b. München - DE | Represented by: Johannes Heselberger |
| 2) | **Cisco Systems, Inc.**<br>(Defendant) - 170 West Tasman Dr. - 95134 - San Jose, CA - US | Represented by: Johannes Heselberger |

PATENT IN DISPUTE

| *Patent no.* | *Holder* |
|---|---|
| **EP2201740** | Lionra Technologies Ltd. |

ADJUDICATING BODY

This decision was pronounced with the participation of the presiding judge Klepsch, the legally qualified judges Dr Schilling as rapporteur and Agergaard as well as the technically qualified judge Dr Keller.

OBJECT

Action for infringement and action for annulment

ORAL HEARING

11 December 2024

BRIEF SUMMARY OF THE FACTS

The plaintiff claims that the defendants 1) and 2) have infringed the European patent EP 2 201 740 B1 ("patent-in-suit") on the territory of the Federal Republic of Germany, which protects, among other things, fast packet switching in a wireless network. The parties are disputing the legal validity of the patent, which the plaintiff is defending in the alternative with a limited defence.

The plaintiff is a company based in Ireland that licences patent portfolios to third parties. Its worldwide portfolio of industrial property rights includes, in particular, inventions in the field of wireless communication and wireless data transmission in communication networks.

Defendant 2) is a US company in the telecommunications industry, Defendant 1) is its German subsidiary. Defendant 2) offers various network solutions such as routers, switches (LAN, SAN), WLAN, network management and security (firewall, authentication, virtual private network). It is the manufacturer of the attacked designs and coordinates their worldwide distribution in close co-operation with its national distribution companies. Defendant 1) displays the attacked designs on the German homepage operated by it. Distribution activities of the two defendants in Germany are disputed between the parties.

Defendant 2) is the manufacturer of the switches in the "Catalyst 9000" product family. Network switches are devices that are used to distribute data streams. They simplify the shared use of resources by connecting all devices - including computers, printers and servers - in a company network. The connected devices can share information and communicate with each other via the switch, regardless of where they are located in a building or on a campus, for example. The information is "packaged" in data packets. In addition to the actual information (payload), these data packets also contain source and destination addresses that are used to forward the packet. For this purpose, each device in the network has a unique, unchangeable hardware address (MAC address). When a packet arrives, the switch checks the destination IP/MAC address and only forwards the packet to the port that matches the destination address.

The plaintiff is registered as the (sole) proprietor of the European patent EP 2 201 740 B1 B1 (patent in suit), granted in English, relating to a "FAST PACKAGE PROCESSING IN A WIRELESS NETWORK" (see patent in suit ("KPS") in
Annex K 4). The patent in suit relates to arrangements for wireless networks. In particular, it relates to a method and a device for high-speed wireless communication.

Processing of protocol headers in an intermediate and/or destination node of a packet-based communication network.

The application on which the patent in suit is based was filed by Harris Corporation on 11 September 2008 and published on 30 June 2010. The patent claims a US priority from 14 September 2007. The reference to the grant of the patent was published on 24 August 2011. The patent in suit is in force in Germany (extract from the register in Annex K 6). The patent in suit has not undergone any opposition or nullity proceedings. It is written in English.

The plaintiff has argued that the patent in suit was transferred within the group on 27 January 2017 and on 1 September 2021, which is disputed between the parties.

The teaching of the patent in suit relates to the reduction of the so-called latency time, i.e. the delay time during packet transmission.

Claim 6 of the patent-in-suit claims a product claim and claim 1 claims a method claim. This arrangement essentially represents a cross-layer architectural framework. This concept is intended to enable a high data transfer rate by enabling the exchange of information protocol layers. In this way, the processing latency is to be reduced and the bandwidth increased.

Claims 1 and 6 of the patent in suit, as granted, read as follows:

> 1. A method for processing a packet at an egress end user node (110), comprising: decoding a packet having a plurality of headers; and subsequent to said decoding step, communicating a portion of said packet to a direct memory access-DMA-device (120); and subsequent to said communicating step, concurrently writing (1) each of said plurality of headers to a packet buffer memory (122) and (2) each individual one of said plurality of headers to a respective protocol stack layer memory (126, 128, 130, 132, 134) where it is available for immediate processing within a protocol stack layer.
>
> 6. An egress end user node (EEUN) (110) of a packet based communications system (100), comprising: a decoder (116) configured for decoding a packet having a plurality of headers; and a direct memory access-DMA-device (120) coupled to said decoder (116) and configured for concurrently writing (1) each of said plurality of headers to a packet buffer memory (122) and (2) each individual one of said plurality of headers to a respective protocol stack layer memory (126, 128, 130, 132, 134) where it is available for immediate processing within a protocol stack layer.

and in German:

> 1. A method of processing a packet in an end-user output node (110), comprising: decoding a packet having a plurality of headers; and subsequent to the decoding step, transmitting a portion of the packet to a

direct memory access DMA device (120); and subsequent to the transmitting step, simultaneously writing (1) each of the plurality of headers into a packet buffer memory (122) and (2) each of the plurality of headers into a corresponding protocol stack layer memory (126, 128, 130, 132, 134) in which it is available for immediate processing within a protocol stack layer.

6. An end-user output node (EEUN) (110) of a packet-based communication system (100), comprising: a decoder (116) adapted to decode a packet having a plurality of headers; and a direct memory access DMA device (120) coupled to the decoder (116) and adapted to simultaneously write (1) each of the plurality of headers into a packet buffer memory (122) and (2) each of the plurality of headers into a corresponding protocol stack layer memory (126, 128, 130, 132, 134) in which it is available for immediate processing within a protocol stack layer.

The plaintiff's allegation of infringement is directed against network switches of the Cisco Catalyst 9x00 series, in particular those with at least one Cisco Unified Access Data Plane (UADP) chip (hereinafter "attacked embodiments"). In this respect, the plaintiff refers to a data sheet (Annex K 8) and a white paper (Annex K 9).

The plaintiff asserts a direct infringement of claim 6 and an indirect infringement of claim 1 of the patent in suit. In the infringement proceedings, it has introduced auxiliary requests ("in particular"), which are based on the respective auxiliary requests to amend the patent, with which it defends the patent-in-suit in the alternative in a limited manner.

MOTIONS BY THE PARTIES

In its reply, the applicant has updated its requests and supplemented them with requests asserted in the alternative, which are based on an alternative limited defence of the patent pursuant to R. 30.1 (a) RP. With regard to the revocation counterclaim and in response to the local division's assessment of the legal status, it has reserved the right to raise one of the requests asserted here "in particular" as the main request.

The applicant claims that the Court should,

I. order the defendants to pay the costs,

1. to refrain from doing so,

a) in the Federal Republic of Germany, to offer, on the market, use, or introduce or possess for said purposes end-user output nodes of a packet-based communication system, each comprising: a decoder to decode a packet having a plurality of headers; and a direct memory access DMA device connected to said decoder for decoding a packet having a plurality of headers.

and is adapted to simultaneously write (1) each of the plurality of headers to a packet buffer memory and (2) each of the plurality of headers to a corresponding protocol stack layer memory in which it is available for immediate processing within a protocol stack layer,

*in particular*

Cisco Catalyst 9x00 series network switches that contain at least one Cisco Unified Access Data Plane (UADP) chip;

(direct infringement of claim 6 of EP 2 201 740 B1)

*especially if*

the end-user output node is further designed to process the multitude of headers in each of the multitude of protocol stack layers simultaneously;

(direct infringement of claim 6 of EP 2 201 740 B1 in the version of auxiliary request 1 in the proceedings for a declaration of invalidity)

*especially if*

the plurality of headers includes a Media-Access-Control layer protocol header and a Network layer protocol header;

(direct infringement of claim 6 of EP 2 201 740 B1 in the version of auxiliary request 2 in the proceedings for a declaration of invalidity)

*especially if*

the protocol stack layers  designed as firmware;

(direct infringement of claim 6 of EP 2 201 740 B1 in the version of auxiliary request 3 in the invalidity proceedings)

*especially if*

the end-user output node is further adapted to simultaneously process the plurality of headers in each of the plurality of protocol stack layers, wherein the plurality of headers comprises a media access control layer protocol header and a network layer protocol header;

(direct infringement of claim 6 of EP 2 201 740 B1 in the version of auxiliary request 4 in the invalidity proceedings)

*especially if*

the plurality of headers comprises a media access control layer protocol header and a network layer protocol header, wherein the protocol stack layers are designed as firmware;

(direct infringement of claim 6 of EP 2 201 740 B1 in the version of auxiliary request 5 in the invalidity proceedings)

*especially if*

the end-user output node is further designed to process the plurality of headers in each of the plurality of protocol stack layers simultaneously, wherein the plurality of

headers comprises a media access control layer protocol header and a network layer protocol header, whereby the protocol stack layers are designed as firmware;

(direct infringement of claim 6 of EP 2 201 740 B1 in the version of auxiliary request 6 in the invalidity proceedings)

b) in the Federal Republic of Germany, offer for use in or deliver to the Federal Republic of Germany end-user output nodes of a packet-based communication system suitable for use in the following method: a method of processing a packet in an end-user output node, comprising: decoding a packet having a plurality of headers; and subsequent to the decoding step, transmitting a portion of the packet to a direct memory access DMA device; and in the decoding step, transmitting a portion of the packet to a direct memory access DMA device: decoding a packet having a plurality of headers; and subsequent to the decoding step, transmitting a portion of the packet to a direct memory access DMA device; and subsequent to the transmitting step, simultaneously writing each of the plurality of headers into a packet buffer memory and each of the plurality of headers into a corresponding protocol stack layer memory in which it is available for immediate processing within a protocol stack layer;

*in particular*

if the end-user output nodes are contained in Cisco Catalyst 9x00 series network switches that include at least one Cisco Unified Access Data Plane (UADP) chip;

(indirect infringement of claim 1 of EP 2 201 740 B1)

*in particular if the process further comprises*

Simultaneous processing of the multitude of headers in each of the multitude of protocol stack layers;

(indirect infringement of claim 1 of EP 2 201 740 B1 in the version of auxiliary request 1 in the proceedings for a declaration of invalidity)

*especially if*

the plurality of headers includes a Media-Access-Control layer protocol header and a Network layer protocol header;

(indirect infringement of claim 1 of EP 2 201 740 B1 in the version of auxiliary request 2 in the proceedings for a declaration of invalidity)

*especially if*

the protocol stack layers designed as firmware;

(indirect infringement of claim 1 of EP 2 201 740 B1 in the version of auxiliary request 3 in the invalidity proceedings)

*in particular if the process further comprises*

simultaneously processing the plurality of headers in each of the plurality of protocol stack layers, wherein the plurality of headers includes a media access control layer protocol header and a network layer protocol header;

(indirect infringement of claim 1 of EP 2 201 740 B1 in the version of auxiliary request 4 in the invalidity proceedings)

*especially if*

the plurality of headers comprises a media access control layer protocol header and a network layer protocol header, wherein the protocol stack layers are designed as firmware;

(indirect infringement of claim 1 of EP 2 201 740 B1 in the version of auxiliary request 5 in the invalidity proceedings)

*in particular if the process further comprises*

simultaneously processing the plurality of headers in each of the plurality of protocol stack layers, the plurality of headers comprising a media access control layer protocol header and a network layer protocol header, wherein the protocol stack layers are configured as firmware;

(indirect infringement of claim 1 of EP 2 201 740 B1 in the version of auxiliary request 6 in the invalidity proceedings)

2.

to impose the following periodic penalty payments to be paid to the court in the event of a breach of the order pursuant to Section I.1:

a) a penalty payment of EUR 10,000 for each sale of a product in the Federal Republic of Germany;

b) a penalty payment of EUR 10,000 for each import of a product into the Federal Republic of Germany;

c) a penalty payment of EUR 10,000 per day of Internet advertising or per advertising brochure handed out to customers in German or English in the Federal Republic of Germany;

3.

to provide the plaintiff with complete information on the extent to which they (the defendants) have committed the acts referred to in section I.1. since 24 September 2011, stating

a) the origin and distribution channels of the infringing products

b) the quantities produced, manufactured, delivered, received or ordered and the prices paid for the infringing products

c) the identity of all third parties involved in the manufacture or distribution of infringing products

d) the prime costs broken down according to the individual cost factors and the profit realised

whereby

e) the list containing the data on the provision of information must also be transmitted in an electronic form that can be analysed by computer;

f) whereby copies of the corresponding purchase and/or order documents (namely invoices, alternatively delivery notes, most alternatively customs documents) must be submitted as proof of the information, whereby details requiring confidentiality outside the data subject to disclosure may be blacked out;

4.

(only defendant 1:) to recall the marketed products referred to in section I.1. above vis-à-vis the commercial customers with reference to the judicially determined infringing condition of the item and with the binding undertaking to reimburse any fees and to bear any necessary packaging and transport costs as well as customs and storage costs associated with the return and to take back the products;

5.

(only the defendant to 1:) to permanently remove the products referred to above in section I.1. from the distribution channels, in which the defendant to 1), with reference to the judicially determined patent infringing condition of the item, requests third parties who are commercial customers but not end customers to cancel all orders relating to the products referred to in section I.1. and to submit written proof to the court and the plaintiff within 30 days of service of the notification within the meaning of R.118(8) sentence 1 VerfO. R.118(8) sentence 1 of the Implementing Regulation and to submit written proof of the action taken;

6.

(only defendant 1:) to hand over the products described under I.1. its direct or indirect possession or in its ownership to a bailiff to be appointed by the plaintiff for the purpose of destruction;

7.

award the plaintiff provisional damages to cover the anticipated costs of the damages proceedings on the plaintiff's side, whereby we leave the specific amount to the discretion of the court;

8.

to provide adequate security for the costs of the legal dispute until the oral hearing; II. to declare that the defendants are jointly and severally liable to compensate the plaintiff for all damages incurred and to be incurred by Harris Corporation in the period from 24 September 2011 to 26 January 2017, by Harris Solutions NY, Inc. (from: 17 April 2018: Harris Global Communications, Inc.) in the period from 27 January 2017 to 29 September 2021 and by the plaintiff since 30 September 2021 as a result of the acts referred to in section I.1.

III. Orders the defendants to pay the costs.

IV. The judgement is immediately enforceable.

V. In the event that security is ordered, to allow the applicant to provide it by means of a bank or savings bank guarantee and to set partial securities for each of the claims recognised and the basic decision on costs.

The defendants request,

I. The plaintiff's application for the provision of security for the costs of the legal dispute (application under I.7) is rejected.

II. The action is dismissed (R. 23, 24 lit. g) VerfO).

III. The defendants are provisionally awarded the reimbursement of costs for the infringement action (R. 150.2 VerfO).

With the counterclaim for a declaration of nullity, they apply:

IV. The European patent EP 2 201 740 is declared invalid with effect for the Federal Republic of Germany to the extent of the asserted claims 1 and 6 (R. 25 VerfO).

V. The defendants are provisionally awarded reimbursement of the costs of the counterclaim (R. 150.2 VerfO).

VI. The court orders the plaintiff to provide security in the amount of EUR 400,000.00, or alternatively security in another appropriate amount, for the costs of the legal dispute and the other costs incurred and to be incurred by the defendants (R. 158.1 VerfO).

In the event that the plaintiff does not provide this security within the time limit set, a default judgement is issued (R. 158.5, 355.1(a) VerfO).

VII. The defendants are released from the obligation to translate the English-language documents submitted as attachments, as well as excerpts reproduced from them, into German (R. 7.1 VerfO in conjunction with R. 24 lit. j) and R. 25 lit. g) VerfO.

The applicant claims that the Court should,

I. The counterclaim for annulment is dismissed.

II. In the alternative, claims 1 and 6 of European patent EP 2 201 740 are given the scope of one of the auxiliary requests 1 to 6 (in numerically ascending order) with effect for the Federal Republic of Germany.

III. The counterclaimant is ordered to pay the costs.

The defendants dispute the plaintiff's entitlement to bring an action, in particular with regard to the two transfer transactions presented.

The defendants deny that the challenged embodiments make use of the teaching of the patent in suit. The Cisco Catalyst 9x00 series switches are not a means which to an essential element of the invention and which is suitable and intended to be used for the use of the invention, Art. 26(1) EPC. The challenged embodiments also did not realise claim 6 of the patent in suit.

To prove the non-patent-compliant design of the challenged embodiments, the defendants rely on the testimony of Mr[redacted] regarding the defendant 2) together with his written declaration as Annex BP 7, as well as the obtaining of an expert opinion.
They also argue that neither defendant has standing. Neither the defendant 1) nor the defendant 2) themselves sell the contested designs in Germany, nor have they sold or delivered them in Germany since 24 September 2011. In this respect, they rely on the testimony of Dr. [redacted] Managing Director/Senior Corporate Counsel of Defendant 1), to be summoned[redacted] this, together with his written statement as Annex BP 8.

With regard to any further motions and further submissions in the written proceedings and in the interim proceedings, reference is made to the parties' written submissions.

KEY PROCESS STEPS

By order dated 1 November 2024, the judge-rapporteur rejected the reciprocal applications for the provision of security for legal costs (ORD_59510/2024).

By order dated 20 November 2024, the Board decided to hear the infringement action and the counterclaim together (ORD_48185/2024).

FACTUAL AND LEGAL ISSUES BETWEEN THE PARTIES

The plaintiff directs its allegation of infringement against network switches which, in its opinion, are offered by the defendant 1) in Germany, "including those of the so-called Cisco Catalyst 9000 family". In particular, network switches of the Cisco Catalyst 9x00 series, which contain at least one Cisco Unified Access Data Plane (UADP) chip, are attacked. These are advertised on the company's website as "modular switches for medium and large campus core networks". It considers the defendant 2) to be responsible for distribution in Germany.

With regard to its active legitimacy, the plaintiff relies on its registration as patent proprietor.

With regard to the allegation of patent infringement, the plaintiff referred to the Cisco Catalyst 9600 Series Switches Data Sheet (Annex K 8) and the Cisco Catalyst 9600 Series Architecture Whitepaper (Annex K 9). These two annexes K8 and K9 describe switches of the Cisco Catalyst 9600 series. It also submitted a statement (private expert opinion) from[redacted] (Annex K 10) and a Cisco presentation "Cisco IOS XE & ASIC Architecture - Catalyst 9000 series" from [redacted] in Annex K 11. August 2024, it subsequently submitted the publication (in excerpts) of [redacted]"Design principles for packet parsers", Architectures for Networking and Communications Systems, [redacted]2013, pp. 13-24 (Annex K 12). In addition, the

Applicant for a video of the presentation "Programmable ASICs for Catalyst Switches" by Muhammad Imam, Manager Technical Marketing.
The defendants deny that the challenged embodiments make use of the teaching of the patent in suit. .

The defendants argue that the Cisco Catalyst 9x00 series switches  not a means relating to an essential element of the invention which is suitable and intended to be used for the use of the invention, Art. 26(1) EPC. The challenged embodiments also did not realise claim 6 of the patent in suit.
With regard to any further motions and further submissions in the written proceedings and in the interim proceedings, reference is made to the parties' written submissions.

REASONS FOR THE DECISION

The admissible action is unfounded. The admissible action for annulment is also unfounded.

A.

The action and the action for annulment are admissible. The jurisdiction of the local division seised is rightly not in dispute between the parties. The plaintiff is authorised to assert the disputed claims arising from the patent in suit (see A. I. below). There are no doubts as to the admissibility of the counterclaim (see A. II. below).

I.

The plaintiff can successfully rely on its registration as proprietor of the patent in suit. 1.

In principle, the active legitimacy for the assertion of annex claims from European patents is based on the substantive entitlement (see BGH, judgement of 7 May 2013 - X ZR 69/11, GRUR 2013, 713, para. 57 et seq. - milling process). Thus, the irrefutable fiction of the applicant's entitlement resulting from Art. 60(3) EPC and Sec. 7 PatG (see Benkard EPÜ/Melullis, 3rd ed. 2019, EPC Art. 60 para. 38) does not apply to the infringement proceedings; its scope of application is limited to the registration proceedings themselves. The entry in the patent register offers no guarantee that its content is correct, as the register has neither a positive publicity effect like the land register nor a negative publicity effect like the commercial register. However, entries in a public register maintained by an administrative authority convey a presumption of correctness and thus a considerable legal appearance (BeckOK PatR/Otten- Dünnweber, 13th ed. 25 July 2019, PatG Section 30 para. 12). The entry in the patent register therefore has a significant indicative effect when assessing the question of who is the substantive owner of the patent (BGH, judgement of 7 May 2013 - X ZR 69/11, GRUR 2013, 713, para. 59 - Fräsverfahren).

2.

Nothing else applies on the basis of the UPCA. According to Rule 8.5 of the Implementing Regulation

> (a) [...] in respect of the proprietor of the European patent, the person who, under the law of the Member State for which the European patent has been granted, is entitled to be registered as proprietor of the patent, irrespective of whether that person is actually registered in the patent register of that Member State (hereinafter referred to as the "national patent register"); and
>
> (b)[..]
>
> (c) For the purposes of paragraph 5, there shall be a rebuttable presumption that the person identified in the relevant national patent register and in the European Patent Register maintained by the European Patent Office is entitled to be registered as proprietor or as applicant, as the case may be.

The Chamber must therefore assume a rebuttable presumption (LK Hamburg, 26 August 2024 - UPC_CFI_54/2023, GRUR-RS 2024, 38164 para. 34 - Avago v. Tesla).
The UPC Court of Appeal has already taken the same approach for patents with unitary effect and assumed that, due to their corresponding entry in the Register for Unitary Patent Protection, this person should be treated as the proprietor of the dispositive patent, Rule 8.4 RP. As such, he was entitled to request the ordering of corresponding measures, Art. 47(1) UPCA (UPC_CoA 335/2023, order of 26 February 2024, p. 24). The provision therefore reverses the burden of presentation and proof with regard to the presumed fact. If the plaintiff can refer to its registration in the relevant registers for the respective legal dispute, it is up to the defendant to demonstrate and, if necessary, prove that the plaintiff lacks the entitlement to such registration (LK Düsseldorf, 30 April 2024 - UPC_CFI_463/2023 - 10x Genomics, Inc. v. Curio Bioscience Inc., LK Hamburg, GRUR-RS 2024, 38164 para. 34 - Avago v. Tesla).

3.

The defendants claim that it is completely unclear whether the patent in suit - which, according to the plaintiff's submission, was transferred twice - was actually the subject of the patent purchase agreement of 27 January 2017. They deny with ignorance that the patent-in-suit, including the annex claims, was effectively transferred from Harris Corp. to Harris Solutions NY, Inc. and the existence of the patent purchase agreement dated
27 January 2017 as such. The alleged transfer had not been entered in the register of the German Patent and Trade Mark Office during the alleged period. The further patent purchase agreement had only been submitted in redacted form. The plaintiff had relied on the certificate of Mr[redacted] for payment of the purchase price. This was already insufficient from a formal point of view, as the plaintiff had not attached a written witness statement to the statement of claim, contrary to Rule 24(j) of the Rules of Procedure. Moreover, it would be expected that the payment of the purchase price could be proven without further ado on the basis of written documents (transfer receipts, etc.). In addition, the alleged transfer on 2 October 2021 and the register status of the DPMA differ considerably. The applicant's change of ownership from Harris Global Communications, Inc. to the applicant is dated 6 February 2023, which again suggests that the alleged original transfer was not effective.

4.

With this submission, the defendants have not successfully challenged the presumption of ownership in accordance with the above principles. The application on which the patent in suit is based was filed by Harris Corporation on 11 September 2008. A change of ownership from Harris Corporation to Harris Global Communications, Inc. is noted in the extract from the register. The defendants have not that Harris Corporation changed its name to L3Harris Technologies, Inc. effective 28 June 2019 and that Harris Solutions NY, Inc. changed its name to HARRIS GLOBAL COMMUNICATIONS, INC. effective 17 April 2018, as alleged by the plaintiff. Nor have they denied that they are affiliated companies, with the result that the first patent transfer agreement of 27 January 2017 took place within the group. The subsequent transfer to the plaintiff is also noted in the register; extracts of the contract have been submitted. The assertion that the purchase price may not have been paid is pure speculation in light of the fact that the transfer was registered on 16 March 2023 (see register excerpt in Annex K 6 and patent purchase agreement in Annex K 5).

II.

There are no concerns regarding the admissibility of the counterclaim. 1.

In particular, the UPC also has international jurisdiction. Pursuant to Article 32(1)(e) UPCA, the UPC has exclusive jurisdiction for counterclaims for revocation of (European) patents. Since there is currently no opt-out (Art. 83 (3) UPCA) from the exclusive jurisdiction of the court in relation to the patent in dispute in force, the UPC - as the common court of the member states of the UPCA - has international jurisdiction for the present counterclaim pursuant to Art. 24 (4), 71a (2) (a), 71b (1) of Regulation (EU) No. 1215/2012.

2.

The plaintiff's requests for alternative amendment of the patent in suit pursuant to R. 30 VerfO are also admissible and in particular in due time filed have been filed in due time. A necessity, "complete" sets of claims cannot be derived from the UPCA or its Rules of Procedure. In some cases, the subject-matter of the amendments is the raising of dependent claims, which means that they are accordingly omitted as additional claims, leaving no doubt as to their further fate. Insofar as it may not be sufficiently clear what the fate of sub-claims 3, 4 and 5 should be, this is not relevant to the decision here (see B. III. 3. g) and D. V.). The plaintiff has already addressed any substantive connections between claims 1 and 6, in particular the question of whether they closed sets of claims, by requesting the corresponding amendments in claims 1 and 6, in each case side by side.

3.

Insofar as the defendants have requested in their reply that further prior art be admitted as an extension of the counterclaim, this request must be granted. It is true that the plaintiff, in its reply in the infringement proceedings, has reorganised, or at least supplemented, its interpretation and the allegation of infringement compared to the statement of claim.

has. Since the plaintiff now no longer refers to the ingress FIFO alone with regard to the "DMA device", but to a combination of several components of the attacked switches, which in turn is to be admitted as a reaction to the defendant's statement of defence, the defendants are to be allowed to introduce the four further prior art documents submitted (Annexes BP-CR5 to BP-CR8) and the statements based on them into the proceedings. In this respect, the Local Division exercises its discretion to the effect that the defendant cannot be criticised for not having already submitted these documents with the counterclaim for a declaration of invalidity due to a lack of knowledge of the plaintiff's supplementary infringement argumentation.

B.

The patent in suit and the auxiliary requests introduced in the plaintiff's reply to the action for revocation must first be interpreted.

I.

According to paragraph [0001], the patent in suit relates to a method and an apparatus for fast processing of protocol headers at an intermediate and/or end node of a packet-based network. It explains in paragraphs [0003] and [0004] that in a packet-based network, the actual application data is preceded by one or more headers which are used to transport the application data within the network. The headers contain data which define, for example, to whom the user data is addressed, where it comes from, what length it has, etc. In accordance with common practice (ISO/OSI reference model), the patent in suit assigns the headers to the layers as follows (see Fig. 2): *Layer-1: PHYSICAL headers, Layer-2: MAC and LLC headers, Layer-3: NETWORK headers, Layer-4: TRANSPORT headers, Layer-5: APPLICATION headers.*

Before the user data of a packet can be processed, e.g. video data can be displayed, the header data must be processed. The patent-in-suit assumes that the header data in known systems has so far processed *sequentially*, i.e. one after the other, layer by layer. This is illustrated in Fig. 5 of the patent in suit. As described in paragraphs [0005], [0006] and [0050] to [0052] of the patent in suit, the packet data was first written sequentially to the packet buffer memory 520 and then passed to the corresponding layer-specific protocol memories 526, 528, 530, 532, and 534. The layer-3 header could only be forwarded after the layer-2 headers had been processed; the layer-4 could only be forwarded after the layer-3 header had been processed, and so on. According to the patent in suit, this processing of the header data out of the packet buffer 520 leads to a long delay (cf. KPS paras [0005], [0011] and [0053]).

II.

The task of the patent in suit is therefore to overcome the time delay in the processing of data packets and in particular headers, the so-called latency in packet transmission. The patent in suit therefore formulates the following task [0011]:

> [0011] In view of the forgoing, there is a need for a solution to reduce protocol header processing time in a packet-based communications

networks. This solution also needs to be configured to update header fields. The solution further needs to be configured to process protocol headers at a desired speed for a battery powered wireless communications device. In this regard, it should be understood that a battery powered wireless communications device can be a node in a high speed wireless communications system. As such, the battery powered wireless communications device can concurrently act as an intermediate node and a destination node. As such, the roles of the battery powered wireless communications device can alternate and vary based on time or traffic conditions.

[0012] The invention concerns a method for processing a packet at an egress end user node. The method includes a decoding step and a concurrent writing step. The decoding step involves decoding a packet having a plurality of headers. The concurrent writing step is performed subsequent to the decoding step. The concurrent writing step involves concurrently writing (1) each of the headers to a packet buffer memory and (2) each individual one of the headers to a respective protocol stack layer memory where it is available for immediate processing within a protocol stack layer.

In the telecommunications environment, "latency" refers to the time it takes for information or a data packet to travel from its source to its destination. It is made up of various delay times caused, for example, by the intermediate storage of data, the checking of data packets or the propagation time of signals.

To solve the problem, the patent in suit in independent claims 1 and 6 to provide a so-called direct memory access (DMA) device as a component. The direct memory access enables a main processor (CPU) to be left out of the memory operations (see paragraph [0023], last sentence). Thus, direct memory access can reduce processing or latency time in the sense of the task of the patent in suit. In particular, the invention utilises the DMA device to reduce the time associated with sequential processing of the headers by performing some of the necessary steps, namely writing the headers into a memory of the respective protocol layer and the packet buffer, simultaneously instead of sequentially, see paragraph [0012].

Claim 1 and claim 6 can be subdivided into the following features (see statement of claim, p. 22 f. and statement of defence, p. 24 f.):

<u>Claim 1</u>

| Merkma | EN | EN |
|---|---|---|
| 1 | A method for processing a packet at an egress end user node (110), comprising: | A method of processing a packet in an end-user output node (110), comprising: |
| a | decoding a packet having a plurality of headers; and | decoding a packet comprising a plurality of headers; and |

| | | |
|---|---|---|
| b | subsequent to said decoding step, communicating a portion of said packet to a direct memory access-DMA-device (120); | following the decoding step, transmitting a portion of the packet to a direct memory access DMA device (120); |
| c | and subsequent to said communicating step, concurrently writing (1) | and following the transfer step, simultaneous writing (1) |
| aa | each of said plurality of headers to a packet buffer memory (122) and | from each of the multitude of headers into a buffer memory (122) |
| bb | (2) each individual one of said plurality of headers to a respective protocol stack layer memory | and (2) of each of the plurality of headers into a corresponding protocol stack layer memory (126, 128, 130, 132,134), |
| (α) | where it is available for immediate processing within a protocol stack layer. | in which it is available for immediate processing within a protocol stack layer. |

Claim 6

| Feature | EN | EN |
|---|---|---|
| 6 | An egress end user node (EEUN) (110) of a packet based communications system (100), comprising: | An end-user output node (EEUN) (110) of a packet-based communication system (100), comprising: |
| a | a decoder (116) | a decoder (116), |
| aa | configured for decoding a packet having a plurality of headers; and | which is adapted to decode a packet comprising a plurality of headers; and |
| b | a direct memory access-DMA-device (120) | a direct memory access DMA device (120), |
| aa | coupled to said decoder (116) and | which [is] coupled to said decoder (116) and |
| bb | configured for concurrently writing (1) | configured for concurrently writing (1) |
| (1) | each of said plurality of headers to a packet buffer memory (122) and | each of the multitude of headers into a packet buffer (122) and |
| (2) | (2) each individual one of said plurality of headers to a respective protocol stack layer memory (126, 128, 130, 132, 134) | (2) of each of the plurality of headers is formed into a corresponding protocol stack layer memory (126, 128, 130, 132, 134), |

| | | |
|---|---|---|
| (α) | where it is available for immediate processing within a protocol stack layer. | in which it is available for immediate processing within a protocol stack layer. |

III.

Claims 6 and 1 of the patent in suit require interpretation with regard to some of their features.

1.

According to the case law of the UPC Court of Appeal, the following principles must be assumed in accordance with Art. 69 of the Agreement on the Grant of European Patents (EPC) and the Protocol on its Interpretation (Protocol on its Interpretation) (UPC_CoA 335/2023, order of 26 February 2024, GRUR-RS 2024, 2829 - NanoString/10x Genomics (detection method), p. 26/27):

> The patent claim is not only the starting point, but also the decisive basis for determining the scope of protection of a European patent. The interpretation of a patent claim does not depend solely on its exact wording in the linguistic sense (see also the English and French language versions of the interpretation protocol: "the strict, literal meaning of the wording used in the claims", "sens étroitet littéral du texte des revendications"). Rather, the description and the drawings must always be used as explanatory aids for the interpretation of the patent claim and not only to resolve any ambiguities in the patent claim. However, this does not mean that the patent claim merely serves as a guideline and that its subject matter also extends to what, after examination of the description and drawings, appears to be the patent proprietor's request for protection.
>
> The patent claim is to be interpreted from the perspective of the person skilled in the art.
>
> When applying these principles, appropriate protection for the patent proprietor should be combined with sufficient legal certainty for third parties.
>
> These principles for the interpretation of a patent claim apply equally to the assessment of infringement and the legal validity of a European patent. This follows from the function of the patent claims which, under the European Patent Convention, to define the scope of protection of the patent under Art. 69 EPC and thus the rights of the patent proprietor in the designated Contracting States under Art. 64 EPC, taking into account the conditions for patentability under Art. 52 to 57 EPC (see EPO GBK, 11 December 1989, G 2/88, OJ 1990, 93 para. 2.5).

2.

The responsible specialist is categorised by the local chamber as graduate engineer specialising in electrical engineering with several years of experience in the field of electrical engineering.

Development of hardware for packet packet processing for packet-based communication networks.

3.

The interpretation of the features of claim 1 is essentially undisputed between the parties, except for the interpretation and classification of feature 1 "Method for processing a packet in an end-user output node (110)". The product claim according to claim 6 is almost identical and is not discussed separately by the parties.

a)

The parties rightly agree that the node according to feature 1, which is to have a function in relation to the data, is located on the consumer side of the data transfer. Insofar as the parties dispute whether only an end node or also an intermediate node is claimed, the Local Court follows the broad interpretation of the plaintiff. This is because, according to the broad description of the application in the introduction to the patent application [para. 0001], the subject matter of the invention is not limited to pure end nodes:

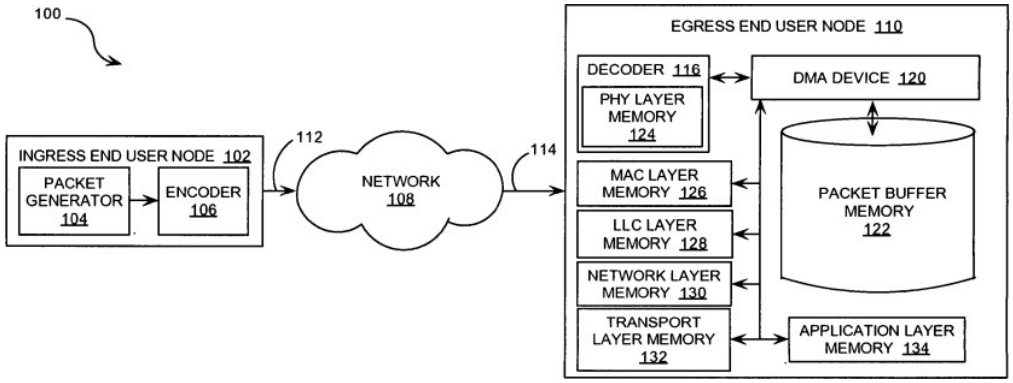
> The inventive arrangements relate to wireless networks. More particularly, the present invention relates to a method and apparatus for high speed protocol header processing at an intermediate and/or destination node of a packet-based communications network.

This does not result in a restriction to pure end nodes; on the contrary, both are expressly disclosed. Both positionings are also taken up again and explained in paragraph [0021]:

> The network 108 is electrically or optically connected to the EEUN 110 via a network link 114. The EEUN 110 is an intermediate or destination node. If the EEUN 110 is a destination node, then the EEUN 100 is the destination of a plurality of packets in a network. The EEUN 110 can be a destination computer system, a routing device, a battery powered wireless communications device, or any other device having a TCP/IP based packet interface.

It is true that the patent specification does not contain any further specific explanation of an intermediate node. However, due to the comparable functionality and the comparable structure, it is clear to the person skilled in the art that it is irrelevant for the teaching of the patent in suit whether a pure target node or a network-immanent distribution node is configured, because an end node can also used as an intermediate node. The term EEUN therefore appears to the person skilled in the art as a generic term for end and intermediate nodes alike.

Contrary to the defendant's view, the opposite cannot be inferred from Figure 4, according to which the EEUN may be connected to the network only electrically or optically, and would thus be part of the packet-based communications network 100, but not part of the network 108 [0019]:




A distinction or separation between the packet-based communication network and the communication system cannot be inferred from the patent application. A justification for such a separation is also not apparent. The "network cloud" in Figure 1 merely reveals to the skilled person that the EEUN receives the packet from the IEUN via a network connection, in contrast to a point-to-point line, because the skilled person is clearly dealing with packet-based communication:

b)

The interpretation of feature 1. a), "decoding a packet comprising a plurality of headers", is not in dispute between the parties. It is undisputed that it concerns the conversion of a coded format back into the original character string in the field of information technology. According to feature 1. a), the object of such an operation is a data packet comprising a plurality of headers. The term header refers to additional data at the beginning (or "head") of a data block that is stored or transmitted. In particular, the data block also contains payload data is therefore a separate header for each layer of the layer protocol.

c)

The interpretation of feature 1. b), "following the decoding step, transmitting a portion of the packet to a direct memory access DMA device (120)", is also not in dispute between the parties. First of all, it is undisputed that, as described in paragraph [0023], a direct memory access DMA device overcomes the disadvantage that normally peripheral devices can typically only transmit data from their memory to a device connected to them by involving the main processor (CPU) of that device. In contrast, there are peripheral devices that transfer data to the device connected to them without the CPU. This process is called direct memory access (DMA) and is performed by a dedicated integrated circuit called a DMA device. The general purpose of a DMA device is to allow peripheral devices to read or write data (to the main memory) without utilising the CPU (Central Processing Unit), para [0023]. This leads to a more efficient use of system resources and improves the overall performance of the computer. The DMA device has the following features

programmable registers or channels for multiple memory operations, see par. [0024]:

> [0024] In general, the DMA device 120 has programming registers for multiple memory transfers. The programming registers are also referred to as DMA channels. In order to choose and uniquely identify a single transfer, a DMA channel is programmed for performing actions to read data from a memory device, to write data to a memory device, to obtain an address for a source memory device, to obtain an address for a destination memory device, and/or to obtain a memory length. The DMA device 120 can also service multiple DMA channels and perform multiple data transfers.

To this end, feature 1. b) teaches, subsequent to the decoding step, transmitting a portion of the packet to a direct memory access DMA device (120). The patent in suit shows this by comparing Figures 5 (prior art, colourisation by the applicant)

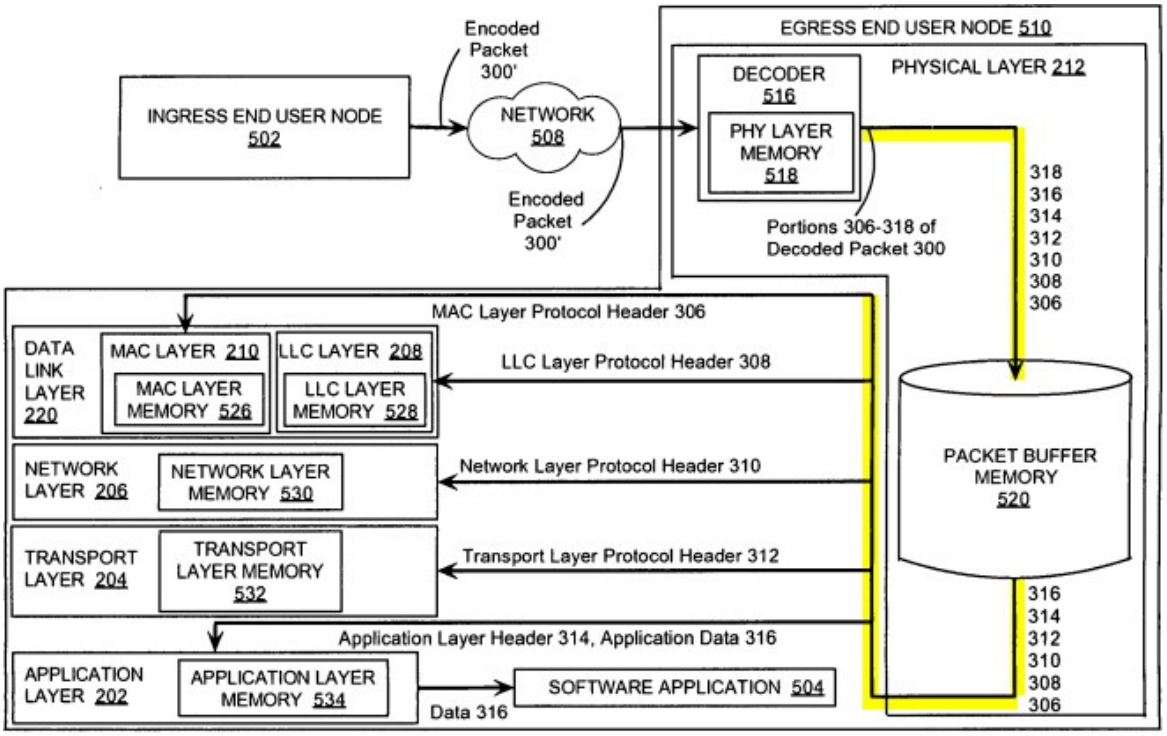
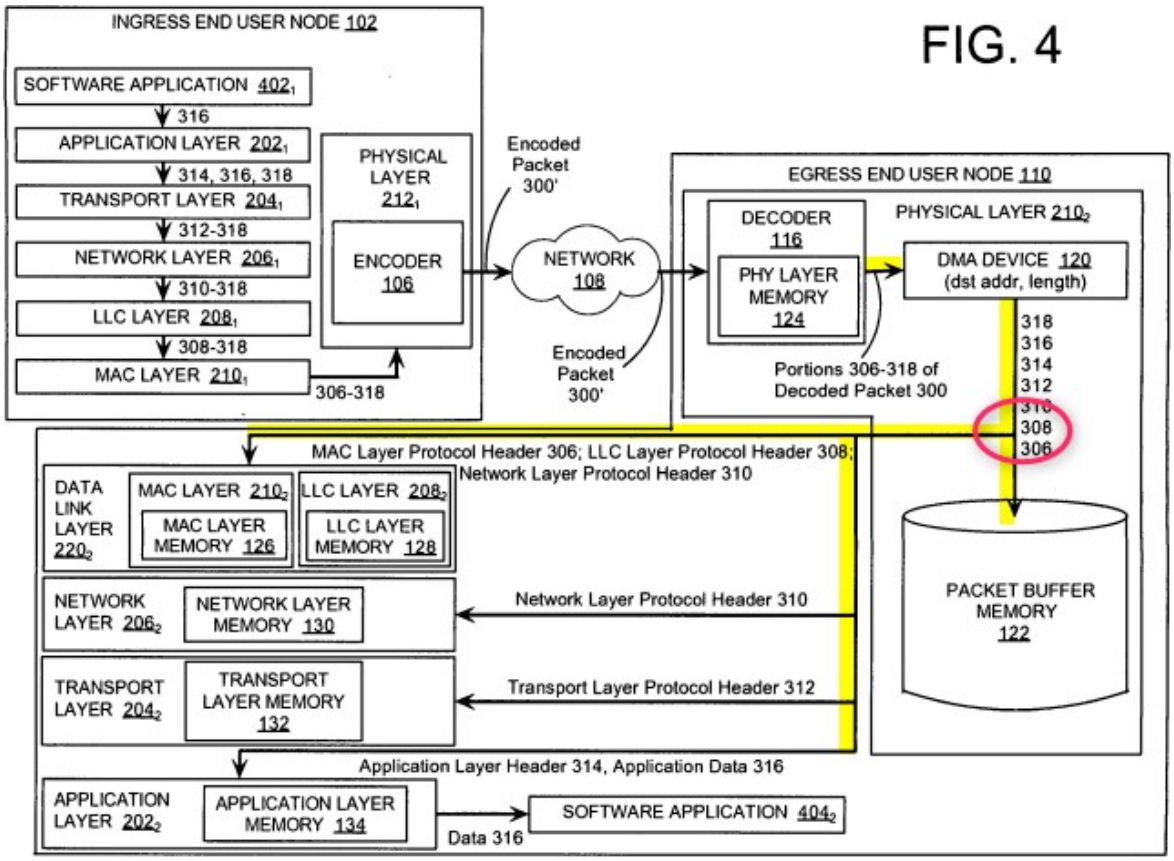



FIG. 5
(PRIOR ART)

and Figure 4 (solution according to the patent in suit, colouring by the plaintiff):




In addition to the receive operation (of the part of the packet) described in feature 1. b), it is functionally necessary that the DMA device according to the patent can enable the storage operations described in feature group 1.c) aa-bb, namely simultaneous storage in the packet buffer memory and the layer-specific memories. The DMA device 120 enables *simultaneous* storage or forwarding of the packet data both in the packet buffer memory and the layer-specific memories. The relevant packet data therefore does not first pass through the packet buffer memory before it reaches the layer-specific memories. For this purpose, the DMA device must also have some kind of control logic, since para [0024], as cited, speaks of different programmed channels. This requires a memory interface that contains control logic that enables the targeted writing of data to the target locations in the memory.

However, the defendants correctly point out that the DMA device according to feature 1. b) should *only* receive *part of* the packet. This is the truncation of the preamble and the PHYSICAL header, which in itself takes place before the decoding step, recognisable to the skilled person.

d)

The feature group 1. c) aa-bb (α), "and subsequent to the transmitting step, simultaneously writing (1) each of the plurality of headers into a packet buffer memory
(122) and (2) of each of the plurality of headers into a corresponding protocol stack layer memory (126, 128, 130, 132, 134) in which it is available for immediate processing within a protocol stack layer," the parties are also substantially in agreement that, unlike the previously disclosed

sequential approach, the headers in a packet buffer memory and in the memory in the respective layer of the protocol stack are no longer written one after the other (cf. Figure 5), but simultaneously (Figure 4). According to the patent in suit, the simultaneous writing by the DMA device according to feature 1. c) is to be achieved by the fact that the DMA device, unlike in known EEUNs, not only performs a data transfer into the packet buffer memory (feature 1. c) aa), but also a transfer into the respective layer-specific memories (feature 1. c) bb). In the prior art according to Figure 5, the transfer of the packet data into the packet buffer memory is awaited, and only then is it transferred - out of the packet buffer memory - into the layer-specific memories for processing. In contrast, according to the teaching of the patent in suit, the packet data is immediately available for processing by the respective protocol stack layer due to the simultaneous storage without the diversions via the packet buffer memory in the respective layer-specific memories. The patent in suit speaks of a "cross layer architecture framework":

> [0026] ... However, the DMA devices are provided only for a one time transfer of a packet from the MAC layer memory to a CPU main memory. As will be appreciated, this single transfer does not solve or deal with the varying latencies and the increased processing consequences present in a high speed wireless network.
>
> [0027] In order to solve this problem, a DMA device is used to concurrently write the specific layer header fields directly into: (a) each protocol stack layer's internal memory spaces 126,[...,] 134 to initiate immediate processing; and (b) the packet buffer memory 122. This arrangement provides what is essentially a cross layer architecture framework. This approach facilitates a high data transfer rate by allowing the exchange of information between the protocol stack layers. In doing so, it reduces processing latency and thereby increases bandwidth.

According to the teaching of the patent in suit, this is intended to avoid the latency or delay resulting from processing according to the prior art shown in Fig. 5. At the same time, it is - indisputably - not a condition that the processing with respect to the packet buffer memory on the one hand and the protocol stack layer memories on the other hand should be carried out quasi simultaneously or to nanosecond. Rather, the "immediate" processability required by feature 1. c) bb.(α) is given if the headers are available in readable form in the corresponding layer-specific protocol memories. The subject matter of claim 1 comprises that the header data is "available for immediate processing", but not the processing itself. By writing the header of a particular layer to a designated memory location in the protocol stack layer memory, it is for immediate processing within its protocol stack layer. The specialist thus realises that in order to be able to write the headers to the memory locations intended for their layer, the DMA device (which performs the writing) must know the position of the headers in the packet. The headers are then written unprocessed (one-to-one) to the corresponding protocol stack layer memories so that processing from the protocol stack layer memories can be carried out.

layer storage can be carried out simultaneously. According to paragraph [0046], this processing also includes the extraction of fields from the headers.

e)

Claims 1 and 6 in the version of auxiliary request 1 present no problems of interpretation. They each add the feature of the granted claim 2 to the granted claims, namely claim 1:

> The method according to claim 1, further comprising
>
> concurrently processing said plurality of headers in each of a plurality of protocol stack layers.
>
> Simultaneous processing of the multitude of headers in each of the multitude of protocol stack layers

or in the case of claim 6:

> The egress end user node being further configured to: concurrently processing said plurality of headers in each of a plurality of protocol stack layers.

In particular, feature 1. c) bb (a) provides that the majority of the headers are available in the corresponding protocol memories for immediate processing. In particular, the headers could also processed simultaneously. Claims 1 and 6 of the auxiliary request
1 define that parallel processing of the various headers of a packet takes place. It can be inferred from this that all headers - not just some of them - are processed at the same time or that their processing starts at least at the same time, as explained, for example, in paragraph [0029] of the patent in suit.

f)

Claims 1 and 6, as amended by auxiliary request 2, add the following feature to the claims as granted:

> Wherein the plurality of headers includes a MAC layer protocol header (306) and a network layer protocol header (310).
>
> where the plurality of headers includes a Media-Access-Control-Layer-Protocol header and a Network-Layer-Protocol header.

In this respect, too, the interpretation no difficulties. The applicant can correctly refer to page 14, lines 16 to 19 and p. 12, lines 5 to 9 of the original description for these features. By further limiting it to "MAC layer protocol header" and "network layer protocol header", auxiliary request 2 also further defines the memory and protocol layers, as disclosed in paragraph [0043]:

> The decoder 116 also performs actions to remove the preamble 302 and the physical layer protocol header 304 from the decoded packet 300. The decoder 116 can further perform actions to forward the preamble 302 and the physical layer protocol header 304 to the physical (PHY) layer memory
> 124 for storage. Thereafter, the decoder 116 performs actions to communicate a portion of the decoded packet 300 to a DMA device 120 (described above in relation to FIG. 1). In this regard, it should be understood

> that the portion of the decoded packet 300 includes a media access control protocol header 306 (described above in relation to FIG. 3), a logic link control (LLC) protocol header 308 (described above in relation to FIG. 3), a network layer protocol header 310 (described above in relation to FIG. 3), the transport layer protocol header 312, the application layer header 314, and the application data 316. The portion of the decoded packet 300 may also include the frame check sequence (FCS) 318.

However, there is no reason to restrict these layers to the so-called "L2" and "L3" layers according to the OSI layer model, as the defendants believe, according to the description of the patent in suit.

g)

With regard to auxiliary request 3, the applicant refers in this respect to page 11, lines 7 to 9, 20, 26 and p. 12 lines 1 and 2 of the original description. It argues that the design of the protocol layers as "firmware" makes it possible to adapt them to different header formats. As a result, the device could be flexibly adapted to different header formats, which not possible in many prior art solutions. In the case in dispute, it can be left open whether this auxiliary request 3 is sufficiently clear in view of the fact that, as the defendants criticise, the patent in suit itself gives no indication of what is understood by firmware. "Firmware" is only described as a counterpart to "hardware", see paragraphs [0034] to [0038]. However, this auxiliary request is no longer relevant (see D. V. below).

h)

Auxiliary requests 4 to 6 combine the characteristics of auxiliary requests 1 to 3. In this respect, reference can be made to the above statements.

C.

The defendant's nullity counterclaim is unfounded in view of the prior art documents introduced with the counterclaim, but also in view of the documents introduced with the duplicate. All citations lack the disclosure of an upstream DMA device provided with programmable channels, which executes the write operations in parallel without switching on the CPU according to the patent in suit. Claims 1 and 6 of the patent in suit thus prove to be legally valid.

I.

The publication US patent application 2006/0072564 A1 (Annex BP-CR1/Cornett), published on 6 April 2006, does not conflict with the validity of the patent in suit.

1.

The publication Appendix BP-CR1/Cornett describes a system for accelerated processing of TCP/IP packets in a packet-based network (see paragraphs [0003] and [0004]). It sets itself the task of accelerating memory access in a node of a network (cf. Para. [0005]), whereby by means of a special network interface controller (NIC) and the processing header data and payload data, a

accelerated processing is to be ensured. According to Figure 10 with associated text, packets received with header and payload on the one hand and headers replicated from the packets on the other hand are stored in different memory locations for accelerated processing.

2.

The BP-CR1/Cornett citation does not oppose the novelty of claims 1 and 6 of the patent in suit, since the core of their solution is to separate the header from the rest of the packet (the payload) and to store the headers in a space-saving manner and process them via the cache, but not to write *in parallel* to a buffer memory on the one hand and to a protocol layer memory on the other.

a)

It cannot be inferred from the citation that parallel storage of the header according to feature group 1. c) takes place and that these headers are then immediately available for further processing. In particular, no *parallel* writing to a buffer memory on the one hand and to a protocol layer memory on the other hand is disclosed. In contrast, no DMA engine is mentioned when storing packets and replicated headers in different memory locations according to Figure 10, so that simultaneity is at least not immediately apparent in the storage operations according to Figure 10. Although the payload contains a large number of headers from higher protocol layers (feature 1. c) aa), according to Figure 10 only 1 header is stored with associated text and no large number of headers are stored individually and simultaneously in a corresponding protocol stack layer memory (feature 1c bb) for immediate processing within the protocol stack layer (feature 1c bb (α)). Rather, the embodiment teaches to store a part of a packet and a header of a packet in the same memory, namely the memory of a CPU.

b)

The paragraph [0034] of the citation cited by the defendants also does not actually prove parallel writing, but merely a split between header and payload, i.e. the actual data content. According to the descriptive passages in paragraphs [0034 and 0036], the header data of a packet is written to two memories. In particular, paragraph [0035] discloses that the header is stored once separately from the payload and once with the payload, but this is done using the CPU:

> [0035] In another embodiment, header 230 may additionally be stored in the second buffer. In an embodiment, this may result from using the split header feature, and placing the header in the same location in which the payload is stored. In other embodiments, this may result from using a header replication feature. In header replication, circuitry may store the header and the payload (i.e., the packet) at a first location (e.g., second buffer), and store a predetermined number of bytes of the packet in a second location (e.g., first buffer). The predetermined number may correlate to a number of bytes of the header in a packet, and may be configurable. With header replication, circuitry does not need to perform parsing to determine where the header ends and the payload begins.

Contrary to the defendant's view, parallel writing is not disclosed by the fact that the network interface controller (NIC 600) must have identified the header data in a first step before writing, e.g. by parsing, in order to be able to store it separately from the user data. The fact that the different protocol stack layer memories (one for each header) do not in fact have to be physically separate memories, which may also apply to the packet buffer memory on the one hand and the plurality of protocol stack layer memories on the other, is also not a requirement. This is because the central element of the teaching of the caveat is that the data is loaded from the CPU memory into a cache memory.

c)

It is true that the use of a DMA device is expressly described in claim 13 of the specification:

> 13. a system comprising:
>
> a chipset having a DMA (direct memory access) engine, the chipset communicatively coupled to a transport protocol driver of a processor and to a network controller; and circuitry to: receive a packet having a payload portion and a header portion; store the packet in a first location, and storing the header portion in a location different from the first location; and determine if the packet is an offload packet, and if the packet is an offload packet, perform accelerated processing on the packet.

For memory operations according to feature group 1. c), however, the citation does not disclose a patent-compliant DMA device in this respect either. Rather, the memory operations are performed solely by a CPU. Contrary to the defendant's view, the NIC is also not described with the task of parallel and direct storage without the CPU. Rather, paragraph [0064] describes that the separation of header and payload enables more storage of headers in the working memory:

> [0064] By splitting a packet apart and excluding packet payloads from these pages, a larger number of headers can be concentrated together. This reduced set of pages can then be managed in a way to permit effective prefetching of packet headers into the processor cache before the protocol stack processes the header.

Nothing else applies to the passage that describes a DMA:

> [0074] For packets selected for splitting, the controller can cause storage 704 (e.g., via Direct Memory Access (DMA)) of the packets header in the page(s) used to store headers and separately store 706 the packet's payload.

These passages also confirm that the memory operations are carried out by a CPU alone and not by bypassing it - in accordance with the patent in suit.

II.

The publication US Patent 7,218,632 (Annex BP-CR2/Bechtolsheim), published on 15 May 2007, also does not conflict with the validity of the patent in suit.

1.

The BP-CR2/Bechtolsheim publication describes a method and a system packet processing in which a router or a switch is able to process incoming packets quickly and perform routing services and other services in real time. A so-called packet processing engine (PPE) receives packets, stores the packets, separates the header and payload by parsing and forwards the header information to a so-called forwarding unit (FFE) for routing decisions. The packet processing engine (PPE) and forwarding unit (FFE) have separate hardware so that their functions can be executed in parallel. It sets itself the task of simplifying complex processing steps. It is proposed to separate the header and user data in the PPE and to leave the decision on their forwarding to a forwarding unit (FFE) (cf. Sp. 1, lines 51 to 61). The header and user data are separated in such a way that the entire packet, i.e. header and user data, is stored in the PPE's memory. The PPE then forwards the header data and the entire packet (i.e. header and user data), as shown schematically in Figure 1.

2.

The citation BP-CR2/Bechtolsheim does not oppose the novelty of claims 1 and 6 of the patent in suit.

a)

It cannot be inferred from the citation that parallel storage of the header would take place, in particular no parallel writing to a buffer memory on the one hand and a protocol layer memory on the other. According to the teaching of this publication, the storage operations of the entire packet and the split header data are not performed in parallel, but sequentially. The entire packet is first stored in the PPE memory and then the header data is split off. In this respectthe storage operations are not performed in parallel. The header information is clearly forwarded and stored after the packet has been stored and parsed; the two storage operations are therefore not simultaneous (feature 1. c).

b)

Furthermore, there is no indication that at least two different protocol layers are available to the headers for immediate and therefore parallel processing. It  true that the caveat describes that the header data and the entire packet (i.e. header and user data) are stored in "two storage locations" in the packet memory. The defendant's assumption that there must necessarily be a switch functionality that routes the header data to one storage location and the entire packet to another storage location, which is different from the storage location of the header data, and that the packet data must be stored in "two storage locations" in the packet memory, is not justified.

and the header data is therefore written "simultaneously" to the respective memories, there is no support for this in the citation. On the contrary, packet is not forwarded to the PPE memory without a CPU. In this respect, it cannot be inferred from the citation that the memory operations described there were carried out by means of a DMA device according to the patent in suit; a DMA device is not mentioned in the publication.

III.

The publication of US patent application 2004/0039787 A1 (Annex BP-CR3/Zemach), published on 26 February 2004, also does not conflict with the legal validity of the patent in suit.

1.

BP-CR3/Zemach describes procedures and devices, such as routers or switches, for processing packets in a network. Several processing resources are used for parallel packet processing, which accessed using DMA techniques. Figure 2 and the associated text describe how a packet processor works. A packet is received via an interface and a first part of the packet is stored in a global packet buffer. A second part of the packet with information required for packet processing, in particular header data, is forwarded to a distributor. The distributor then forwards part of the packet to an available packet processing engine. After processing, a further modified part of the packet is stored in an output packet header buffer and then this modified part of the packet, together with the part in the global packet buffer, is forwarded as a modified packet to the next component. The latter in particular a sequential processing approach, from which the patent in suit seeks to distinguish itself.

2.

The citation BP-CR3/Zemach does not oppose the novelty of claims 1 and 6 of the patent in suit.

a)

The citation lacks a disclosure of the parallel write operations according to the patent in suit. It is true that Figure 2 of BP-CR3/Zemach shows a switch in which two lines (arrows) lead away from the input interface circuit, one into the distributor 220 and one into the packet memory. However, contrary to the defendant's view, this publication does not teach that the write operation to the input memory of the distributor 220 would occur *simultaneously* with the write operation to the global packet memory 239.

b)

Furthermore, it is not recognisable that the input interface circuit 212 according to feature
1. b) of the patent in suit only receives part of the package. Rather, according to the solution in the publication, the entire package is received. Unlike in the patent teaching of the patent in suit, no direct processing takes place in the "distributor 220" ("distributor"), so that the distributor cannot represent a protocol layer memory . The

In any case, the assumed input memory of the distributor does not constitute a protocol stack layer memory in accordance with the patent in suit, into which a plurality of headers can be written individually and simultaneously in accordance with their protocol, so that they are available for immediate processing within the protocol stack layer. Although the publication also discloses a division of packets into overlapping header and payload parts, no division of received or decoded packets within the meaning of feature groups 1. a) - b) is disclosed in accordance with the patent in suit.)

c)

Furthermore, according to the teaching of the patent in suit, the decoder and the DMA are separate units, since the patent in suit requires a transmission from the decoder to the DMA. This is not disclosed in the BP-CR3/Zemach citation.

Moreover, there is nothing to suggest that the input interface circuit (212) could constitute a DMA and would have a read and write device with control logic. In this respect, it must be taken into account that the publication recognises DMA devices in principle, but does not use them for the purposes of write and store operations. Rather, a DMA according to this publication is only provided at the point of processing according to paragraph [0040]:

> [0040] FIG. 3C illustrates one embodiment of a packet processing engine 365. processor 382, based on instructions provided by instruction cache 381, performs operations on the Second Subset of bytes of a received packet and/or other data or information stored in data memory 383. Data memory is one type of computer-readable medium. In one embodiment, packet-processing engine 365 communicates with other components and/or resources via direct memory access (DMA) device 384, although any communication mechanism could be used.

IV.

The publication US Patent 6,687,247 (Annex BP-CR4/Wilford), published on 3 February 2004, also does not conflict with the validity of the patent in suit.

1.

BP-CR4/Wilford describes an architecture for high-speed routing of packets in a network. After reception, demodulation, deframing and processing of the received packets, the packets are received via an interface according to Figure 8 with associated text and then both the packets are stored in a packet memory, which is designed as a FIFO, and the headers are stored in a lookup header FIFO.

is written. The header data is then written to the lookup header FIFO as shown in Figure 8 "parsed".

2.

The citation BP-CR4/Wilford does not oppose the novelty of claims 1 and 6 of the patent-in-suit, since it does not disclose a protocol stack layer memory or a DMA according to the patent-in-suit.

a)

It is not apparent from the citation that the lookup header FIFO there is to be understood as a protocol stack layer memory according to the patent in suit, in which a plurality of headers, here MAC and IP headers, are written individually and simultaneously in each case according to their protocol layer (feature 1.c.bb) for direct processing within the respective protocol stack layer (feature 1.c.bb.(α)). Instead, the headers written in the lookup header FIFO must first be parsed in order to be available individually for processing according to their protocol layer and then sent to the lookup CORE.

b)

A DMA according to the patent in suit is also not disclosed in the publication. Although a DMA device is mentioned in the publication, it is not mentioned in connection with write operations in the packet memory FIFO or lookup header FIFO (feature 1.b). Whether and at what specific point in the packet processing a division, in particular of the preamble and physical layer header, of received or decoded packets takes place is also not apparent from the citation. Contrary to the view of the defendant, no DMA device within the meaning of feature 1. b) can therefore be regarded as disclosed in the "Physical Layer Interface Module (PLIM)".

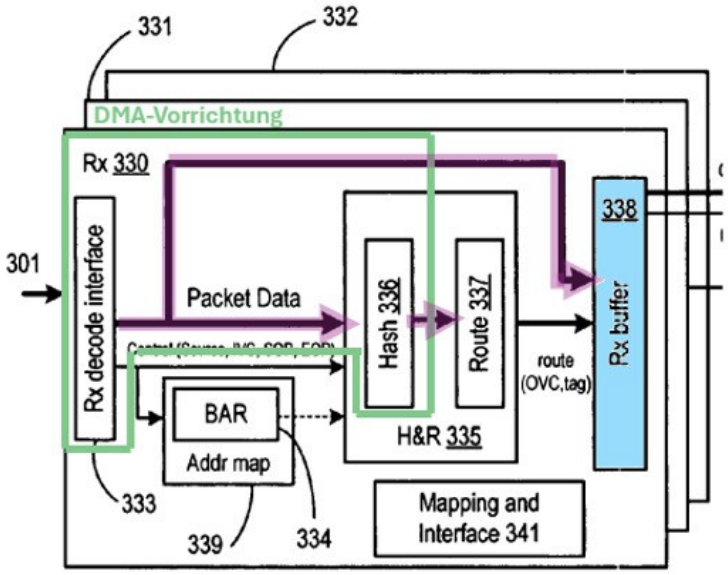
V.

The US patent application 2005/0078601 A1 (Annex BP-CR5/Moll), published on 14 April 2005, also does not conflict with the legal validity of the patent in suit.

1.

The BP-CR5/Moll describes a multiprocessor switching chip for parallel routing of packets in high-speed networks. According to Figure 3, a decoder decodes received packets and forwards packet data to a receiver buffer for storage as well as packet data and header data to a so-called hash and route circuit. One of these

included hash block extracts fields, especially headers, from the package and "hashes" them them if required (see Figure 3 with colouring of the defendant):




2.

Even taking into account the optionality of the hash operation in block 336, the citation BP-CR5/Moll does not oppose the novelty of claims 1 and 6 of the patent in suit, since no DMA according to the patent in suit is disclosed.

a)

Irrespective of how the green line in defendant's colouring in Figure 3 is drawn, the citation does not disclose a DMA in accordance with the patent in suit, but only a simple data line. This is because in BP-CR5/Moll the header data is transmitted as a block, which must first be fed to the parser, here the hash block 336. According to paragraph [0081] of the citation, the packet data contains all headers and the payload. In contrast, according to the teaching of the patent-in-suit, only a portion of the packet is transmitted to the direct memory access DMA device after the decoding step, whereas prior to transmission, the preamble and the physical layer header are already stored separately and are therefore not included in the portion of the packet that is transmitted to the DMA device. According to the teaching of BP-CR5/Moll, however, this is the task of the decoder, namely to transmit the packet data without the preamble and PHYSICAL header to the Rx buffer and to the H&R circuit.

b)

The citation further does not disclose that the individual headers would be written to respective protocol stack layer memories from where they would be available for immediate processing within the respective protocol stack layer. Rather, specific parts of the headers are used as part of an input set for a hash function and mapped to a common hash value, as disclosed in paragraphs [0051 and

0052] show. The headers for the subsequent "routing block 337" are therefore not separately separate processing within a protocol stack layer. c)

Even from the point of view that the hash operation according to paragraph [0051] is only to be implemented optionally, there is no disclosure that the individual headers would be written after decoding (in parallel) into respective protocol stack layer memories, from where they would be available for immediate processing within the respective protocol stack layer. Rather, contrary to the view of the defendant, there is no disclosure for the subsequent
"routing block 337" does not provide the headers separately for separate processing within a protocol stack layer. This only provides a simple data line, which still requires subsequent parsing of the header data. According to paragraph [0081] of the citation, the headers are only separated by downstream processing in hash block 336.

d)

In addition, no decoding is disclosed and subsequently the transfer to a DMA device, which then writes the headers simultaneously to two different memories. The disclosure of a DMA device in the citation has a different purpose, namely a packet manager, as para [0029] shows:

> [0029]. The packet manager 148 circuitry communicates packets between the interfaces 162, 166, 170 and the system memory, and may be a direct memory access (DMA) engine that writes packets received from the Switching module 140 into input queues of the System memory and reads packets from output queues of the System memory to the appropriate configurable packet-based interface 162, 166, 170. The packet manager 148 may include a packet manager input and a packet manager output each having its own DMA engine and associated cache memory. The cache memory may be arranged as first in first out (FIFO) buffers that respectively support the input queues and output queues.

VI.

Finally, US Patent 7,069,372 B1 (Annex BP-CR6/Leung), published on 27 June 2006, does not conflict with the validity of the patent in suit.

1.

The BP-CR6/Leung describes a processor with an array pipeline with a plurality of programmable stages for processing packets for a router with a plurality of input and output ports for packets. Referring to Figures 2 and 3, received packets are first stored in one of a plurality of packet FIFO buffers. A packet arbiter selects a packet and forwards it to a so-called header sequencer. This header sequencer forwards the entire packet to a packet buffer memory and extracts the packet header and forwards it to a parsing processing unit.

unit (PXU). According to Figure 14, the parsing processing unit (PXU) parses the packet header to extract the IP destination address.

2.

The citation BP-CR6/Leung does not oppose the novelty of claims 1 and 6 of the patent-in-suit, since it does not disclose a direct memory access DMA device either.

a)

A memory or buffer is not described in the citation for the parsing processing unit (PXU). Thus, the document does not disclose a protocol stack layer memory according to the patent (features 1.c.bb or 6.b.bb.(2)), in which a plurality of headers are written individually and simultaneously according to their protocol layer for immediate processing within the respective protocol stack layer (features 1.c.bb.(α) or 6.b.bb.(2).(α)). Instead, only the IP header is forwarded to the parsing processing unit (PXU) and parsed there without intermediate storage and then forwarded directly to a lookup execution unit (LxU), in which the lookup process takes place with the help of the array pipeline. DMA techniques with regard to write operations between the receive interface and the global packet buffer as well as the distributor are not mentioned in the publication (features 1.b or 6.b). No direct memory access DMA device is disclosed that performs parallel writing of headers to a buffer memory on the one hand and a protocol layer memory on the other hand.

b)

Nor can the version of Figure 2 of BP-CR6/Leung coloured by the defendants show a "DMA device" designed in accordance with the patent in suit, because the DMA itself would then carry out the header separation (parsing), which would not be in accordance with the claim, and because there is in any case no simultaneous and not sequential storage of the headers in two memory locations. Moreover, the operations are carried out by the CPU and not bypassing it, which according to the teaching of the patent in suit is supposed to be the essence of a DMA device.

VII.

The other caveats -[redacted] and[redacted] (Annex BP-CR7/Cisco) and
P. Crowley et al. (Exhibit BP-CR8/NPD) - are also not capable of opposing the novelty of claims 1 and 6.

1.

The BP-CR7/Cisco is an extract, pages 147 to 165, from the reference book by[redacted] a[redacted] entitled "Cisco LAN Switching Fundamentals: The essential guide for understanding Ethernet switched networks", which was published by Cisco Press in 2004. This book excerpt describes the Catalyst 6500 switch architecture and the multilayer switching process. In some places in the publication, in particular on pages 158 and 162, it is mentioned that Layer 2 and Layer 3 layer headers are processed simultaneously within the protocol stack layer (added feature according to auxiliary request 1). However, the publication does not disclose a direct storage layer according to the patent in suit.

access DMA device (features 1.b or 6.b) and also no protocol stack layer memory according to the patent in suit (features 1.c.bb or 6.b.bb.(2)).

2.

BP-CR8/NPD is an excerpt, pages 191 to 218, from the reference book by [redacted] et al. entitled "Network Processor Design" from 2003. In this excerpt, the publication describes the necessity and various possible applications of programmable network processors (NP). The network processors are described there as programmable microprocessors that have been optimised for packet processing through modifications. The functionality of the network processors is provided, among other things, by corresponding microcode, which can also be referred to as firmware (added feature according to auxiliary request 3).

In particular, this very general document does not disclose a direct memory access DMA device (features 1.b or 6.b) or a protocol stack layered memory (features 1.c.bb or 6.b.bb.(2)) according to the patent in suit.

VIII.

The defendants have also not been able to successfully deny the existence of the required inventive step. All the printed documents lack the disclosure of a DMA at the early point in accordance with the patent in suit. There was no reason for the person skilled in the art to include a DMA in accordance with the patent in suit in these self-contained solutions.

1.

According to Art. 56 p. 1 EPC, an invention is considered to an inventive step if it is not obvious to a person skilled in the art from the prior art. This inventive solution begins beyond the area which, based on the state of the art, is defined by what the skilled person with average knowledge, skill and experience can routinely develop and find in the relevant technical field (see Benkard/Söldenwagner, EPC, 4th ed., Art. 56 para. 9). An invention is deemed to exist if it does not result from the usual approach of the person skilled in the art, but requires an additional creative effort on their part (LK Düsseldorf, 3 August 2024 - UPC CFI 7/2023, GRUR-RS 2024, 17732 para. 93; LK Hamburg, 26 August 2024 - UPC CFI 54/2023, GRUR-RS 2024,
38164 para. 135 - Avago v. Tesla).

2.

With regard to the claimed combination of document BP-BP- CR7, it is not apparent why the skilled person should be required to combine it with BP-CR7 on the basis of BP-CR5. BP-CR5 deals with packet switching within a multi-processor device, whereas BP-CR7 deals with a multi-layer switch. Moreover, BP-CR5 calculates a hash value to perform routing, while BP-CR7 proposes L2 and L3 engines. These approaches are based on a different approach, which is why the specialist has no reason to combine the self-contained solution of BP-CR5 with BP-CR7. Moreover, even with an assumed combination, the specialist would

of the two documents does not reach the claimed subject matter, since the further Characteristics 1. b), 1. c) bb. and 1. c) bb (α) are not shown to the skilled person in the BP-

CR7. 3.

With regard to the claimed combination document BP-CR6 with document BP-CR7, it is also not clear why the skilled person should be required to combine them. BP-CR6 shows a "systolic array" for sequential processing of a packet, while BP-CR7 proposes L2 and L3 engines. These approaches are also based on a different approach, which is why the expert had no reason to replace the solution of one with that of the other. Moreover, the skilled person did not arrive at the claimed subject-matter even with an assumed combination of the two documents, since features 1. b) and 1. c) bb. (α) are not shown to the skilled person in BP-CR7 either.

IX.

claims 1 and 6 as granted proved to be legally valid, the condition for the auxiliary requests introduced by the applicant under Rule 30 VerfO did not materialise. The question of the patentability of the auxiliary requests can therefore be left to one side.

D.

The infringement action is unfounded. The indirect patent infringement of claim 1 of the patent in suit alleged by the plaintiff pursuant to Art. 26 (1) EPC does not exist. In any case, there is no literal realisation of feature 1. b) and feature group 1. c) aa-bb by the attacked embodiments. Accordingly, there is also no direct infringement of claim 6 pursuant to Art. 25 UPCA.

I.

The plaintiff directs its allegation of infringement against network switches which, in its opinion, are offered by the defendant 1) in Germany, "including those of the so-called Cisco Catalyst 9000 family", in particular network switches of the Cisco Catalyst 9x00 series, which contain at least one Cisco Unified Access Data Plane (UADP) chip.

In dispute between the parties is the realisation of features 1., 1. b), 1. c) bb) and Feature 1. c) bb.(α)) by these attacked embodiments.

II.

The starting point is that the Catalyst 9600 series switches are end-user output nodes within the meaning of feature 1 of the patent in suit. The fact that they are intermediate nodes is, as explained, harmless. This is because, according to the broad application description in the introduction to the patent application [para. 0001], the

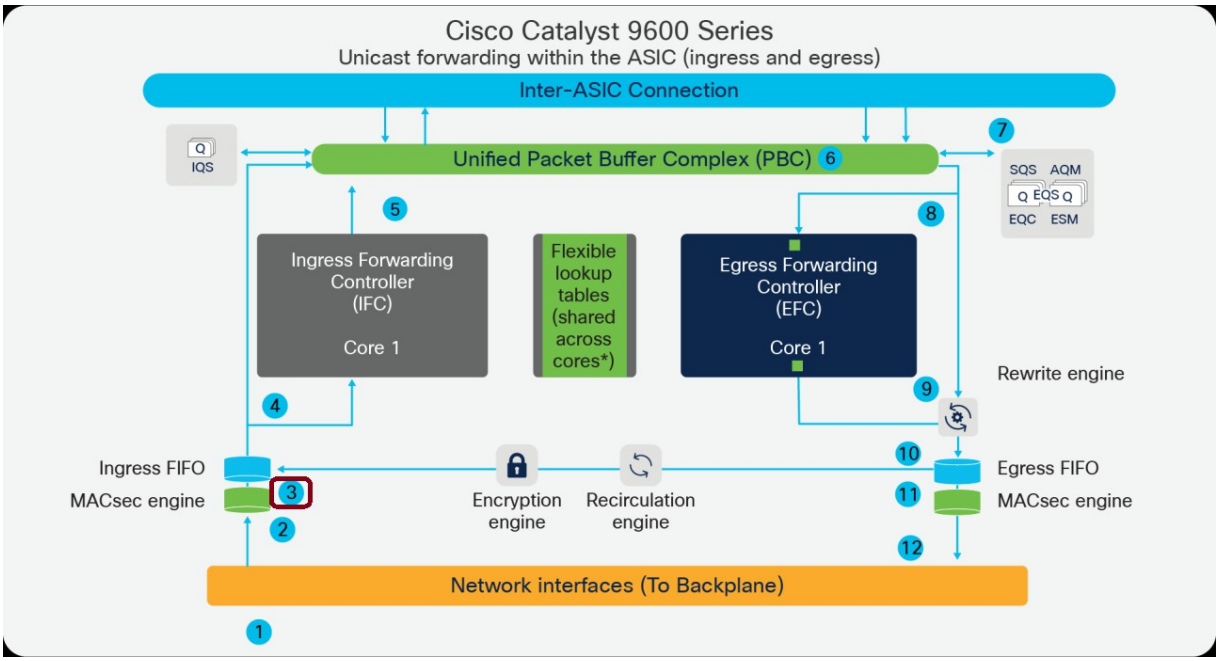
The object of the invention is not limited to pure end nodes. It is decisive, but also sufficient, that data packets are transmitted via them in an Ethernet network.

III.

However, the realisation of feature 1. b) of claim 1 cannot be established either on the basis of the plaintiff's submission in the statement of claim or on the basis of the submission in the reply.

1.

In the statement of claim, the plaintiff the position that the Ingress First In First Out (FIFO) is a direct memory access DMA device within the meaning of the patent in suit because it stores the header information at the desired locations without a diversion via a main processor (see Whitepaper, p. 26, Annex K 9):




She was of the opinion that the data packet from the Ingress FIFO was routed directly to both the PBC and the IFC, i.e. not via a CPU. In view of the extremely high data throughputs that Cisco can achieve with its ASICs according to its specifications, anything else is not realistic; in the expert's view, a DMA device is the only possible technical solution.

2.

The defendants have denied infringement in relation to this feature. They have argued that, according to common knowledge, a DMA device always includes a "control logic" that manages targeted storage in a specific storage location. However, the Ingress FIFO lacks a corresponding control logic. It only outputs data to a data line and has no knowledge of where this data line leads or whether there is a unit at the end of the data line that can process the incoming data at all. For this reason, the Ingress FIFO is also not in the

able to write data. The PBC and the IFC of the challenged embodiments store the data arriving on the data lines in memories managed by these units. The ingress FIFO could not influence this, since - in contrast to a DMA device - it lacked the control logic required for memory addressing in the target memory.

3.

A realisation of feature 1. b) of claim 1, "following the decoding step, transmitting a part of the packet to a direct memory access DMA device (120)," is to be denied according to the above interpretation of the feature.

a)

Functionally, in addition to the receive operation described in feature 1b (of the part of the packet), it would be necessary for the DMA device according to the patent to be able to enable the memory operations described in feature group 1.c) aa-bb, namely simultaneous storage in the packet buffer memory and the layer-specific memories (see also Fig. 4). This requires a memory interface that contains a control logic in the form of programmed registers or channels that enables the targeted writing of data to the target locations in the memory. However, the accused embodiments do not make use of this.

aa)

The figure from the white paper shows a line between Ingress FIFO and IFC and PBC, but not that this could represent a DMA. When interpreting the feature, however, the plaintiff also correctly assumes that the DMA must enable storage and a "naked" data line cannot embody a DMA. However, it is not apparent from the diagram that a control logic could be present in the contested embodiments and not just a data line. The presence of programmed registers or channels is not apparent.

bb)

The statement by Mr[redacted] (Annex K 10), on the other hand, is not able to provide any insight, as he did not examine the switch, but merely assumed that the CPU was not involved because it would otherwise too slow, and that the Ingress FIFO writes header data to two memories.

b)

Furthermore, even according to the plaintiff's submission, it is not possible to recognise that the ingress FIFO receives *part of the packet* as DMA. Rather, it is only the ingress FIFO of the IFC that initially collects parts of the packet. According to the white paper, the fork also takes place

already after the ingress FIFO, whereas according to the teaching of the patent-in-suit it only takes place after the DMA.

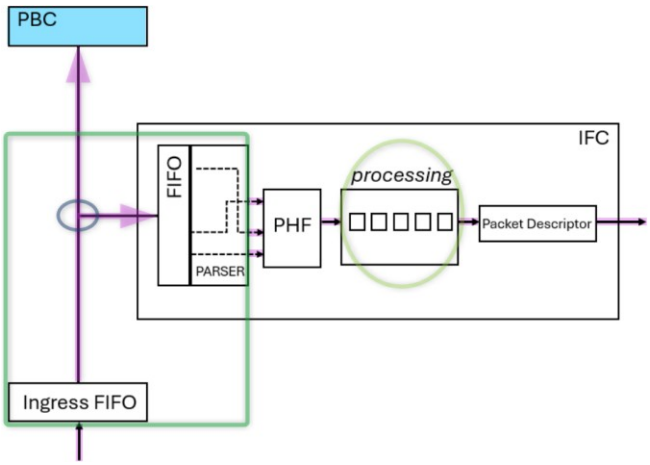
4.

Nor can the realisation of feature 1. b) of claim 1 be established on the basis of the plaintiff's submission in its reply.

a)

In its reply, the plaintiff  the defendants' statements in the statement of defence, according to which the Ingress Forwarding Controller IFC uses the information of the first 256 bytes from the FIFO to make forwarding decisions, including checking the individual packet headers to determine the appropriate output path. For this purpose, the packet is forwarded to a "parser" included in the IFC, as the defendants have schematically argued. Its task is to break down the packet and extract important header information associated with the various protocol layers. It is essential that the 256 bytes are "parsed", i.e. analysed and interpreted, in order to extract the information contained therein, that this information is written to the "PHF data object" (as referred to by the defendants) and that the "PHF data object" is stored in a memory (in this specific case: a register) in which the header data is stored separately according to its affiliation to the various relevant stack layers and the header data  available there for each layer to be called up immediately and therefore quickly accessible and processable.

The plaintiff has presented this schematically as follows (see the plaintiff's reply to the statement of defence, para. 49):




In her opinion, the ingress FIFO also needs to know where the data should go and this is "calculated". The fact that the parser only occurs afterwards is harmless, as the effect is only relevant for the second data line. The patent in suit has no mandatory requirement in this respect, but leaves it  to the skilled person to decide where to do it, with the aim of sequential work. The data streams would also start at the same time; the preamble and L1 layer had already been separated beforehand.

b)

Contrary to the plaintiff's view, the "parser" processing unit in the IFC cannot be assigned to the slam DMA device. aa)

Rather, the IFC is the first storage location, whereby it can remain open whether or not it can represent a protocol stack layer memory within the meaning of feature 1. c) bb, because the data is then written to the next storage location, the so-called "PHF" from the above figure. However, the fact that the parser extracts the header data is one level too late to realise the teaching of the patent in suit, because it would be required that the DMA as the first instance itself performs the writing to two different storage locations. However, even according to the plaintiff's submission, the ingress FIFO does not carry out this writing work, but is ultimately limited to a simple data line that operates on the principle of first-in-first-out. However, a simple data line followed by a control unit (or parser) does not make an ingress FIFO a DMA according to the patent in suit. As the defendants have argued without contradiction, the processing in the parser results in a delay by a factor of 10, which is contrary to the objective of the teaching according to the patent.

bb)

If, on the other hand, the ingress FIFO of the IFC were to be regarded as a functionally integrated part of the DMA device, the distribution to the two storage locations would only take place from there. However, by directly routing the ingress FIFO, the IFC is bypassed on way to the PBC. According to the teaching of the patent in suit, however, separation must take place in advance so that the DMA can write the headers to the correct layer or compartment. This single write operation achieves the desired simultaneity of the write operations. Writing the headers is also distinguished in the patent in suit from processing the fields, cf. para. [0046], in particular also the fields from the headers. In the parser of the challenged embodiments, on the other hand, the processing takes place at a time which, according to the patent in suit, should not yet take place in the interest of saving time.

c)

In addition, the defendants claim that if the ingress FIFO, the FIFO of the IFC *and* the parser contained in the IFC were to form a *uniform* DMA device, they would then also have to realise a control logic which enabled targeted writing to the protocol stack layer memory and to the packet buffer memory (cf. feature group 1. c aa- bb). The DMA device according to the patent in suit has various programmed registers or channels for this purpose according to paragraph [0024]. However, as already explained, there is no  of this in the challenged infringing forms. According to the diagram, the IFC writes to the PBC in the same way as the Ingress FIFO, which has already forwarded to the PBC - without recognisable control logic. It is therefore up to the recipient to allocate the data to the correct area.

IV.

A realisation of feature 1. c) of claim 1 cannot be established either. As already explainedthe challenged embodiments lack that neither the ingress FIFO as alleged DMA nor a DMA combined from ingress FIFO and IFC simultaneously stores the headers in a packet buffer memory and in the memory in the respective packet buffer memory.

layer of the log stack. Furthermore, it is not recognisable in the two forwardings to the PBC that these data records would be stored separately in the sense of the specifications of feature group 1. c). It is true that the Ingress FIFO sends the packet "in parallel" to the Ingress Forwarding Controller (IFC) and the Packet Buffer Complex (PBC) without involving the CPU. However, neither the Ingress FIFO as a supposed DMA nor a DMA combined from Ingress FIFO and IFC simultaneously write the *headers* into a packet buffer memory and into the memory in the respective layer of the protocol stack, as shown in Figure 4 of the patent in suit. Rather, only the first 256 bytes of the packet are written to the input FIFO of the IFC as a single data stream. The respective header is also not immediately available in the memory of the respective stack layer - the IFC - for further processing, but must first be extracted by the parser. Accordingly, the criterion of simultaneity is missing.

V.

The question of the realisation of the characteristics of the auxiliary requests (see the plaintiff's reply to the statement of defence, para. 88 et seq.) can be left to one side, as the main characteristics have not yet been realised.

VI.

For the (lack of) direct infringement of the product claim protected by claim 6, reference can be made to the above statements because the claim is almost identical in wording.

VII.

The question of passive legitimisation is also no longer relevant in the absence of patent infringement. E.

In view of all the above, the infringement action together with its annex requests must be dismissed without further considerations of proportionality pursuant to Article 63 (1) UPCA.

A decision must nevertheless be on the action for annulment.

As part of the decision on costs, the Local Court took into account that the plaintiff was unsuccessful in its entirety with regard to the applications, but that the defendants were unsuccessful with regard to the action for annulment. The plaintiff stated EUR 1.5 million as the amount in dispute for the infringement action. The defendants have not objected to this. The value in dispute of the action for cancellation is subject to a surcharge of up to 50% in accordance with section I. 2. b) (2)
(ii) the "Guidelines of the Administrative Committee for the determination of court fees and the upper limit for recoverable costs of 24 April 2023" (cf. Art. 36 para. 3 UPCA, R. 370.6 UPC Rules of Procedure). The revocation counterclaim is therefore valued at EUR 2.25 million and the proceedings as a whole at EUR 3.75 million.

The defendants' request to award them a provisional reimbursement of costs for the infringement and cancellation counterclaim was not granted. Pursuant to Rule 150.2 of the Rules of Procedure, a provisional reimbursement of costs may be awarded to the successful party in the decision on the merits [Rule 119] or in a decision on the determination of damages under conditions to be determined by the court. Since the defendants have to bear the majority of the costs of the proceedings themselves, a provisional reimbursement of costs was

not indicated. The defendants have not shown that they are dependent on a provisional pro rata reimbursement of costs. In this respect, the parties are to be referred to the regular cost assessment procedure in accordance with Rule 150.1 of the Rules of Procedure.

## DECISION

I. The action is dismissed.

II. The counterclaim is dismissed.

III. The plaintiff is ordered to pay 40% of the costs of the proceedings and the defendants 60%.

IV. The defendant's application for provisional reimbursement of costs is rejected.

V. The total value of the proceedings is set at EUR 3,750,000.

## DETAILS OF THE DECISION

Action Number: ACT 7940/2024 UPC
number: UPC_CFI_58/2023 Action
type: Infringement Action
Related proceedings: CC 33752/2024
Related proceedings type: Counterclaim for revocation

## SIGNATURES

Sabine Maria Klepsch
Digitally signed by Sabine Maria Klepsch
Date: 2025.02.14 13:01:03 +01'00'

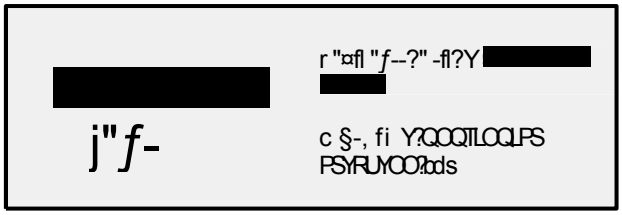
Presiding Judge Klepsch

Stefan Schilling
Digitally signed by Stefan Schilling Date: 2025.02.14 12:19:20 +01'00'

Legally qualified judge Dr Schilling

Peter Juul Agergaard
Digitalt signeret af Peter Juul Agergaard
Dato: 2025.02.14 14:29:39 +01'00'

Legally qualified judge Agergaard



Technically qualified judge Dr Keller

Carolin Bauch

Digitally signed by Carolin Bauch Date: 2025.02.14 15:26:34 +01'00'

for the Deputy Chancellor

INFORMATION ON THE APPOINTMENT

An appeal against this decision may lodged with the Court of Appeal within two months of notification of the decision by any party whose petitions were unsuccessful in whole or in part (Art. 73(1) UPCA, R. 220.1(a), 224.1(a) RP).

INFORMATION ON ENFORCEMENT

A certified copy of the enforceable decision is issued by the Deputy Registrar at the request of the enforcing party (Art. 82 UPCA, Art. Art. 37(2) UPCA, R. 118.8, 158.2, 354, 355.4 VerfO).

This decision was announced at a public meeting on 19 February 2025.

Stefan Schilling

Digitally signed by Stefan Schilling Date: 2025.02.19 10:24:34 +01'00'

Judge with legal qualifications Dr Schilling Rapporteur